Detailed experimental results presented in the paper DPLL(T): Fast Decision Procedures

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The following tables are the extended version of the results presented in the paper *DPLL(T): Fast Decision Procedures*. The tables contain (in their third column) the translation times for four eager approaches: SD and EIJ, and the two hybrid methods Hybrid1 and Hybrid2[1] Furthermore, for two major SAT solvers, zChaff (version 2003.12.04) and BerkMin (its recent version 561) the running times on the translated formulas are given. For easier comparison with our system, the times for zChaff and BerkMin *include* the translation times as well. The choice of zChaff and BerkMin is motivated by the fact that our current DPLL(X) engine is modelled after zChaff and that BerkMin is presently considered one of the best SAT solvers overall. In order to show that the conclusions are independent of the SAT solver used, all experiments have been repeated with two versions of the SAT solver Siege. One can observe that the same conclusions can be derived. The last table is a comparison with SVC (version 1.1) and ICS 2.0.

Results are in seconds, with times greater than 100s rounded to whole numbers. Each system was run on a 2GHz 512MB Pentium-IV under Linux, with exactly the same setting for each benchmark except for the "Two queues" benchmarks where our system had learning (and hence also backjumping and restarts) turned off. Each benchmark was run for 6000 seconds. An annotation of the form (*memory*) in a column indicates that the system timed ran out of memory on the benchmarks, whereas an annotation +6000 indicates that the benchmark could not be solved within 6000 seconds.

[1]For Hybrid2, SEP_THOLD=700 turned out to be the best value, after we tried with 500, 600, 700, 800 and 900.

Family	File	SD	Berkmin	Chaff	DPLL(T)
Buggy Cache Coherence	Bug1	1.58	**1.65**	2.72	5.98
	Bug2	0.71	0.72	0.72	**0.67**
Code Validation Suite	22s	2.54	9.28	9.25	**0.48**
	25s	2.39	4.93	3.83	**0.41**
	27s	0.49	0.52	0.52	**0.27**
	32s	0.5	0.6	0.55	**0.25**
	37s	1.27	1.38	1.39	**0.35**
	38s	0.96	1.04	1.09	**0.35**
	43s	3.05	21.34	21.11	**0.58**
	44s	0.7	1.08	1.36	**0.26**
	46s	1.15	1.48	1.6	**0.29**
	49s	3.19	3.23	3.2	**0.44**
DLX processor	dlx1c	1.25	2.9	3.97	**0.36**
	dlx1c.rwmem	1.35	4.07	4.61	**0.41**
	dlx1c.rwmem1	1.33	3.2	4.71	**0.39**
Elf processor	6steps	0.1	**0.1**	**0.1**	0.21
	7steps	0.64	0.68	0.72	**0.31**
	8steps	1.68	1.73	2.15	**0.5**
	9steps	4.04	9.57	11.73	**1.26**
	10steps	7.45	66	89.78	**6.11**
	12steps	20.21	5804	+6000	**567**
Out of order processor (rf)	6steps	0.49	0.54	0.57	**0.28**
	7steps	0.86	1.22	1.75	**0.4**
	8steps	1.43	4.55	8.72	**0.96**
	9steps	2.15	38.59	102	**2.8**
	10steps	3.24	438	1100	**16.81**
	11steps	4.59	5729	+6000	**92**
	12steps	6.26	+6000	+6000	**859**
	13steps	8.06	+6000	+6000	**5413**
Out of order processor (tag)	8steps	0.87	1.05	1.62	**0.44**
	10steps	2.22	3.38	7.56	**0.93**
	12steps	4.11	8.98	37.46	**3**
	14steps	6.95	25.99	166	**12.52**
	15steps	8.89	**34.65**	404	51.89
	17steps	12.45	**50.89**	348	201
	19steps	18.84	**122**	492	1709
Load-Store processor	6steps	0.24	0.26	0.27	**0.06**
	8steps	0.88	1.31	1.53	**0.41**
	10steps	2.55	5.15	8.79	**1.2**
	12steps	6.3	12.52	45.07	**4.16**
	14steps	12.2	31.04	183	**24.43**
Cache Coherence Protocol	8steps	0.54	**0.54**	**0.54**	0.61
	10steps	0.96	**0.96**	1.05	4.29
	12steps	1.61	**2.06**	2.58	26.33
	14steps	2.45	**22.11**	50.72	83.72
	15steps	2.93	**92.91**	215	163
	16 steps	3.4	**253**	909	377
	17 steps	3.97	846	2455	**794**
	18 steps	4.54	2933	+6000	**2152**
Two queues	10steps	0.48	0.7	0.87	**0.25**
	12steps	0.63	2.02	3.31	**0.4**
	14steps	0.8	5.51	8.56	**0.95**
	18steps	1.45	94.44	406	**14**
	20steps	1.76	304	729	**58**

Family	File	EIJ	Berkmin	Chaff	DPLL(T)
Buggy Cache Coherence	Bug1	4.83	**4.89**	7.82	5.98
	Bug2	1.46	1.53	1.49	**0.67**
Code Validation Suite	22s	10.61	10.76	11.45	**0.48**
	25s	6.24	6.3	6.4	**0.41**
	27s	0.26	**0.26**	0.27	0.27
	32s	0.35	0.36	0.35	**0.25**
	37s	0.42	0.42	0.42	**0.35**
	38s	0.45	0.45	0.45	**0.35**
	43s	2.19	2.23	2.27	**0.58**
	44s	0.27	0.27	0.27	**0.26**
	46s	0.76	0.76	0.77	**0.29**
	49s	19.16	19.24	19.2	**0.44**
DLX processor	dlx1c	3.14	3.35	3.43	**0.36**
	dlx1c.rwmem	4.97	5.34	5.6	**0.41**
	dlx1c.rwmem1	4.88	5.2	5.4	**0.39**
Elf processor	6steps	0.07	**0.07**	**0.07**	0.21
	7steps	0.55	0.55	0.55	**0.31**
	8steps	2.82	2.88	2.87	**0.5**
	9steps	16.71	17.15	17.31	**1.26**
	10steps	memory			**6.11**
	12steps	memory			**567**
Out of order processor (rf)	6steps	0.68	0.69	0.69	**0.28**
	7steps	1.4	1.43	1.48	**0.4**
	8steps	2.74	3.07	3.46	**0.96**
	9steps	4.72	6.7	10.48	**2.8**
	10steps	7.6	27.52	74.32	**16.81**
	11steps	11.74	169	1836	**92**
	12steps	17.45	1244	+6000	**859**
	13steps	24.31	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.39	1.42	1.42	**0.44**
	10steps	4.3	4.77	5.12	**0.93**
	12steps	10.26	13.34	14.6	**3**
	14steps	21.39	38.36	46.58	**12.52**
	15steps	28.95	64.04	72.6	**51.89**
	17steps	53.39	**124.36**	211.65	201
	19steps	90.66	**263.38**	484.78	1709
Load-Store processor	6steps	0.17	0.17	0.17	**0.06**
	8steps	1.2	1.22	1.26	**0.41**
	10steps	5.37	5.72	5.79	**1.2**
	12steps	25.31	26.99	29.63	**4.16**
	14steps	memory			**24.43**
Cache Coherence Protocol	8steps	1.04	1.05	1.04	**0.61**
	10steps	2.88	2.93	**2.9**	4.29
	12steps	7.82	**8.23**	8.71	26.33
	14steps	26.54	**54.7**	85.69	83.72
	15steps	64.1	189.81	338.49	**163**
	16 steps	memory			**377**
	17 steps	memory			**794**
	18 steps	memory			**2152**
Two queues	10steps	2.51	2.8	3.07	**0.25**
	12steps	16.89	25.4	30.47	**0.4**
	14steps	memory			**0.95**
	18steps	memory			**14**
	20steps	memory			**58**

Family	File	Hybrid 1	Berkmin	Chaff	DPLL(T)
Buggy Cache Coherence	Bug1	4.81	4.89	7.76	**5.98**
	Bug2	1.44	1.52	1.46	**0.67**
Code Validation Suite	22s	2.64	2.72	2.72	**0.48**
	25s	2.19	2.23	2.21	**0.41**
	27s	0.25	**0.25**	**0.25**	0.27
	32s	0.25	**0.25**	**0.25**	**0.25**
	37s	0.41	0.41	0.41	**0.35**
	38s	0.4	0.4	0.41	**0.35**
	43s	1.87	1.94	1.97	**0.58**
	44s	0.35	0.35	0.35	**0.26**
	46s	0.72	0.73	0.73	**0.29**
	49s	4.15	4.19	4.16	**0.44**
DLX processor	dlx1c	3.2	3.36	3.92	**0.36**
	dlx1c.rwmem	4.97	5.4	5.69	**0.41**
	dlx1c.rwmem1	4.92	5.3	5.59	**0.39**
Elf processor	6steps	0.1	**0.1**	**0.1**	0.21
	7steps	0.57	0.57	0.57	**0.31**
	8steps	2.73	2.76	2.77	**0.5**
	9steps	9.96	10.27	10.39	**1.26**
	10steps	27.08	31.68	35.95	**6.11**
	12steps	147	896	1596	**567**
Out of order processor (rf)	6steps	0.66	0.67	0.67	**0.28**
	7steps	1.44	1.47	1.5	**0.4**
	8steps	2.56	2.86	3.3	**0.96**
	9steps	4.47	6.33	10.17	**2.8**
	10steps	7.18	25.02	59.55	**16.81**
	11steps	10.84	145	934	**92**
	12steps	15.91	1343	+6000	**859**
	13steps	22.29	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.3	1.34	1.4	**0.44**
	10steps	3.75	4.2	4.68	**0.93**
	12steps	8.96	12.32	13.51	**3**
	14steps	17.89	32.79	40.06	**12.52**
	15steps	24.86	52.54	62.5	**51.89**
	17steps	44.96	**164**	189	201
	19steps	73.72	**345**	488	1709
Load-Store processor	6steps	0.2	0.21	0.2	**0.06**
	8steps	1.23	1.25	1.28	**0.41**
	10steps	4.63	4.82	5.05	**1.2**
	12steps	14.87	16.53	17.77	**4.16**
	14steps	43.18	56.77	64.12	**24.43**
Cache Coherence Protocol	8steps	1.08	1.08	1.08	**0.61**
	10steps	2.89	2.94	**2.91**	4.29
	12steps	7.83	**8.25**	8.71	26.33
	14steps	26.43	**54.49**	85.47	83.72
	15steps	64.43	190	340	**163**
	16 steps	memory			**377**
	17 steps	memory			**794**
	18 steps	memory			**2152**
Two queues	10steps	2.48	2.77	3.04	**0.25**
	12steps	17	25.44	30.65	**0.4**
	14steps	memory			**0.95**
	18steps	memory			**14**
	20steps	memory			**58**

Family	File	Hybrid 2	Berkmin	Chaff	DPLL(T)
Buggy Cache Coherence	Bug1	2.16	**2.28**	2.77	5.98
	Bug2	0.88	0.89	0.89	**0.67**
Code Validation Suite	22s	12.37	12.51	12.92	**0.48**
	25s	7.91	7.98	8.15	**0.41**
	27s	0.28	0.28	0.28	**0.27**
	32s	0.32	0.32	0.33	**0.25**
	37s	0.37	0.37	0.37	**0.35**
	38s	0.4	0.4	0.4	**0.35**
	43s	2.11	2.15	2.19	**0.58**
	44s	0.28	0.28	0.28	**0.26**
	46s	0.88	0.89	0.89	**0.29**
	49s	2.83	2.87	2.84	**0.44**
DLX processor	dlx1c	3.16	3.43	3.59	**0.36**
	dlx1c.rwmem	4	4.84	5.58	**0.41**
	dlx1c.rwmem1	4.18	4.62	5.16	**0.39**
Elf processor	6steps	0.09	**0.09**	**0.09**	0.21
	7steps	0.43	0.44	0.43	**0.31**
	8steps	2.49	2.55	2.54	**0.5**
	9steps	15.67	16.23	16.49	**1.26**
	10steps	7.38	33.49	47.94	**6.11**
	12steps	21.13	3129	5400	**567**
Out of order processor (rf)	6steps	0.56	0.57	0.58	**0.28**
	7steps	1.23	1.26	1.31	**0.4**
	8steps	2.24	2.59	2.86	**0.96**
	9steps	3.83	6.16	10.69	**2.8**
	10steps	5.88	47.31	182	**16.81**
	11steps	8.83	373	1716	**92**
	12steps	12.75	4195	+6000	**859**
	13steps	17.65	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.16	1.18	1.26	**0.44**
	10steps	3.47	3.96	4.25	**0.93**
	12steps	8.19	10.32	13.46	**3**
	14steps	16.56	27.23	48.03	**13.68**
	15steps	22.71	55.9	106	**51.89**
	17steps	34.3	1340	+6000	**201**
	19steps	54.47	5479	+6000	**1709**
Load-Store processor	6steps	0.19	0.19	0.2	**0.06**
	8steps	1.08	1.11	1.14	**0.41**
	10steps	4.77	5.05	5.49	**1.2**
	12steps	21.48	23.62	24.95	**4.16**
	14steps	12.58	**15.5**	15.93	24.43
Cache Coherence Protocol	8steps	0.78	0.78	0.78	**0.61**
	10steps	1.37	**1.37**	1.38	4.29
	12steps	2.51	2.6	**2.59**	26.33
	14steps	4.07	**5.9**	7.96	83.72
	15steps	5.07	**8.98**	29.68	163
	16 steps	6.4	**20.71**	47	377
	17 steps	7.75	**42.18**	227	794
	18 steps	9.39	**126**	374	2115
Two queues	10steps	0.44	0.51	0.56	**0.25**
	12steps	0.68	1.08	1.34	**0.4**
	14steps	0.93	5.22	11.99	**0.95**
	18steps	1.61	141	169	**14**
	20steps	2.08	645	1649	**58**

SUMMARY OF RESULTS (Chaff, BerkMin)

SD

Family	**Berkmin**	**Chaff**	**DPLL(T)**
Buggy Cache Coherence	**2.37**	3.44	6.66
Code Validation Suite	44.88	43.9	**3.68**
DLX processor	10.17	13.29	**1.16**
Elf processor	5882	6104(1 TO)	**575**
Out of order processor (rf)	18211 (2 TO)	19213 (3 TO)	**6385**
Out of order processor (tag)	**247**	1457	1979
Load-Store processor	51.44	239	**30.26**
Cache Coherence Protocol	4151	9634 (1 TO)	**3601**
Two queues	407	1148	**73.6**

EIJ

Family	**Berkmin**	**Chaff**	**DPLL(T)**
Buggy Cache Coherence	**6.42**	9.31	6.66
Code Validation Suite	41.05	41.85	**3.68**
DLX processor	13.89	14.43	**1.16**
Elf processor	12021 (2 MO)	12021 (2 MO)	**575**
Out of order processor (rf)	7453 (1 TO)	13926 (2 TO)	**6385**
Out of order processor (tag)	**510**	837	1979
Load-Store processor	6034 (1 MO)	6037 (1 MO)	**30.26**
Cache Coherence Protocol	18257 (3 MO)	18437(3 MO)	**3601**
Two queues	18028 (3 MO)	18034 (3 MO)	**73.6**

Hybrid 1

Family	**Berkmin**	**Chaff**	**DPLL(T)**
Buggy Cache Coherence	**6.41**	9.22	6.66
Code Validation Suite	13.47	13.46	**3.68**
DLX processor	14.06	15.2	**1.16**
Elf processor	941	1646	**575**
Out of order processor (rf)	7524 (1 TO)	13009 (2 TO)	**6385**
Out of order processor (tag)	**612**	799	1979
Load-Store processor	79.58	88.42	**30.26**
Cache Coherence Protocol	18257 (3 MO)	18438 (3 MO)	**3601**
Two queues	18019 (3 MO)	18028 (3 MO)	**73.6**

Hybrid 2

Family	**Berkmin**	**Chaff**	**DPLL(T)**
Buggy Cache Coherence	**3.17**	3.66	6.66
Code Validation Suite	28.05	28.65	**3.68**
DLX processor	12.89	14.33	**1.16**
Elf processor	3182	5467	**575**
Out of order processor (rf)	10626 (1 TO)	13913 (2 TO)	**6385**
Out of order processor (tag)	6918	12173 (2 TO)	**1979**
Load-Store processor	45.47	47.71	**30.26**
Cache Coherence Protocol	**209**	690	3601
Two queues	793	1832	**73.6**

TO: time out
MO: memory out

Family	File	SD	Siege_v3	Siege_v4	DPLL(T)
Buggy Cache Coherence	Bug1	1.58	**1.63**	1.85	5.98
	Bug2	0.71	0.72	0.72	**0.67**
Code Validation Suite	22s	2.54	5.98	6.43	**0.48**
	25s	2.39	4.05	3.73	**0.41**
	27s	0.49	0.51	0.51	**0.27**
	32s	0.5	0.55	0.56	**0.25**
	37s	1.27	1.36	1.36	**0.35**
	38s	0.96	1.03	1.02	**0.35**
	43s	3.05	15.14	14.31	**0.58**
	44s	0.7	1.22	1.23	**0.26**
	46s	1.15	1.45	1.41	**0.29**
	49s	3.19	3.2	3.2	**0.44**
DLX processor	dlx1c	1.25	3.49	3.2	**0.36**
	dlx1c.rwmem	1.35	5.24	5.52	**0.41**
	dlx1c.rwmem1	1.33	2.9	2.95	**0.39**
Elf processor	6steps	0.1	**0.11**	**0.11**	0.21
	7steps	0.64	0.67	0.67	**0.31**
	8steps	1.68	1.92	1.88	**0.5**
	9steps	4.04	7.55	8.13	**1.26**
	10steps	7.45	40.62	42.33	**6.11**
	12steps	20.21	4936	3532	**567**
Out of order processor (rf)	6steps	0.49	0.52	0.54	**0.28**
	7steps	0.86	1.6	1.69	**0.4**
	8steps	1.43	4.99	5.63	**0.96**
	9steps	2.15	56.74	54	**2.8**
	10steps	3.24	774.76	627	**16.81**
	11steps	4.59	+6000	+6000	**92**
	12steps	6.26	+6000	+6000	**859**
	13steps	8.06	+6000	+6000	**5413**
Out of order processor (tag)	8steps	0.87	1.11	1.07	**0.44**
	10steps	2.22	4.3	4.85	**0.93**
	12steps	4.11	9.07	9.02	**3**
	14steps	6.95	26.1	18.77	**12.52**
	15steps	8.89	**25.2**	28.15	51.89
	17steps	12.45	**42.62**	53.03	201
	19steps	18.84	**79.68**	95.71	1709
Load-Store processor	6steps	0.24	0.27	0.27	**0.06**
	8steps	0.88	1.26	1.21	**0.41**
	10steps	2.55	4.6	4.61	**1.2**
	12steps	6.3	16.41	15.3	**4.16**
	14steps	12.2	33.18	33.05	**24.43**
Cache Coherence Protocol	8steps	0.54	**0.55**	**0.55**	0.61
	10steps	0.96	**0.97**	**0.97**	4.29
	12steps	1.61	**1.87**	1.91	26.33
	14steps	2.45	25.58	**20.89**	83.72
	15steps	2.93	118	**102**	163
	16 steps	3.4	296	**242**	377
	17 steps	3.97	900	921	**794**
	18 steps	4.54	4174	3305	**2152**
Two queues	10steps	0.48	0.73	0.76	**0.25**
	12steps	0.63	2.5	2.44	**0.4**
	14steps	0.8	8.88	8.11	**0.95**
	18steps	1.45	374	237	**14**
	20steps	1.76	1143	610	**58**

Family	File	EIJ	Siege_v3	Siege_v4	DPLL(T)
Buggy Cache Coherence	Bug1	4.83	5.7	**4.9**	5.98
	Bug2	1.46	1.47	1.47	**0.67**
Code Validation Suite	22s	10.61	10.8	10.69	**0.48**
	25s	6.24	6.28	6.28	**0.41**
	27s	0.26	**0.27**	**0.27**	**0.27**
	32s	0.35	0.36	0.36	**0.25**
	37s	0.42	0.43	0.43	**0.35**
	38s	0.45	0.46	0.46	**0.35**
	43s	2.19	2.23	2.22	**0.58**
	44s	0.27	0.28	0.28	**0.26**
	46s	0.76	0.77	0.77	**0.29**
	49s	19.16	19.17	19.17	**0.44**
DLX processor	dlx1c	3.14	3.25	3.25	**0.36**
	dlx1c.rwmem	4.97	5.38	5.6	**0.41**
	dlx1c.rwmem1	4.88	5.11	5.13	**0.39**
Elf processor	6steps	0.07	**0.08**	**0.08**	0.21
	7steps	0.55	0.56	0.56	**0.31**
	8steps	2.82	2.85	2.85	**0.5**
	9steps	16.71	17.25	17.16	**1.26**
	10steps	memory			**6.11**
	12steps	memory			**567**
Out of order processor (rf)	6steps	0.68	0.69	0.69	**0.28**
	7steps	1.4	1.45	1.44	**0.4**
	8steps	2.74	3.07	3.17	**0.96**
	9steps	4.72	7.26	6.62	**2.8**
	10steps	7.6	24.89	27.13	**16.81**
	11steps	11.74	383	253	**92**
	12steps	17.45	+6000	+6000	**859**
	13steps	24.31	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.39	1.42	1.42	**0.44**
	10steps	4.3	5.57	5.29	**0.93**
	12steps	10.26	14.76	12.48	**3**
	14steps	21.39	32.05	31.22	**12.52**
	15steps	28.95	48.32	**45.29**	51.89
	17steps	53.39	**118**	123	201
	19steps	90.66	**180**	530	1709
Load-Store processor	6steps	0.17	0.18	0.18	**0.06**
	8steps	1.2	1.22	1.24	**0.41**
	10steps	5.37	5.77	5.63	**1.2**
	12steps	25.31	28.11	27.5	**4.16**
	14steps	memory			**24.43**
Cache Coherence Protocol	8steps	1.04	1.05	1.05	**0.61**
	10steps	2.88	2.89	**2.89**	4.29
	12steps	7.82	8.15	**8.06**	26.33
	14steps	26.54	**49.67**	51.82	83.72
	15steps	64.1	247	164.35	**163**
	16 steps	memory			**377**
	17 steps	memory			**794**
	18 steps	memory			**2152**
Two queues	10steps	2.51	2.76	2.78	**0.25**
	12steps	16.89	30.26	28.7	**0.4**
	14steps	memory			**0.95**
	18steps	memory			**14**
	20steps	memory			**58**

Family	File	Hybrid 1	Siege_v3	Siege_v4	DPLL(T)
Buggy Cache Coherence	Bug1	4.81	**4.88**	5.79	5.98
	Bug2	1.44	1.45	1.45	**0.67**
Code Validation Suite	22s	2.64	2.71	2.7	**0.48**
	25s	2.19	2.2	2.2	**0.41**
	27s	0.25	**0.26**	**0.26**	0.27
	32s	0.25	0.26	0.26	**0.25**
	37s	0.41	0.42	0.42	**0.35**
	38s	0.4	0.41	0.41	**0.35**
	43s	1.87	1.9	1.91	**0.58**
	44s	0.35	0.36	0.36	**0.26**
	46s	0.72	0.73	0.73	**0.29**
	49s	4.15	4.16	4.16	**0.44**
DLX processor	dlx1c	3.2	3.32	3.52	**0.36**
	dlx1c.rwmem	4.97	5.25	5.29	**0.41**
	dlx1c.rwmem1	4.92	5.18	5.15	**0.39**
Elf processor	6steps	0.1	**0.11**	**0.11**	0.21
	7steps	0.57	0.58	0.58	**0.31**
	8steps	2.73	2.75	2.75	**0.5**
	9steps	9.96	10.31	10.22	**1.26**
	10steps	27.08	30.77	31.35	**6.11**
	12steps	147	1015	+6000	**567**
Out of order processor (rf)	6steps	0.66	0.67	0.67	**0.28**
	7steps	1.44	1.48	1.48	**0.4**
	8steps	2.56	3.03	3.01	**0.96**
	9steps	4.47	6.11	6.32	**2.8**
	10steps	7.18	21.19	25.28	**16.81**
	11steps	10.84	375	266	**92**
	12steps	15.91	+6000	+6000	**859**
	13steps	22.29	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.3	1.32	1.32	**0.44**
	10steps	3.75	4.01	4.07	**0.93**
	12steps	8.96	11.08	11.17	**3**
	14steps	17.89	24.92	30.14	**12.52**
	15steps	24.86	**43.23**	45.38	51.89
	17steps	44.96	102	**91.19**	201
	19steps	73.72	244	**226**	1709
Load-Store processor	6steps	0.2	0.21	0.21	**0.06**
	8steps	1.23	1.25	1.25	**0.41**
	10steps	4.63	4.78	4.8	**1.2**
	12steps	14.87	17.19	16.86	**4.16**
	14steps	43.18	50.18	56.33	**24.43**
Cache Coherence Protocol	8steps	1.08	1.09	1.09	**0.61**
	10steps	2.89	**2.9**	**2.9**	4.29
	12steps	7.83	**8.05**	8.08	26.33
	14steps	26.43	46.24	**45.6**	83.72
	15steps	64.43	177	172	**163**
	16 steps	memory			**377**
	17 steps	memory			**794**
	18 steps	memory			**2152**
Two queues	10steps	2.48	2.85	2.72	**0.25**
	12steps	17	28.73	29.98	**0.4**
	14steps	memory			**0.95**
	18steps	memory			**14**
	20steps	memory			**58**

Family	File	Hybrid 2	Siege_v3	Siege_v4	DPLL(T)
Buggy Cache Coherence	Bug1	2.16	**2.27**	2.56	5.98
	Bug2	0.88	0.89	0.89	**0.67**
Code Validation Suite	22s	12.37	12.55	12.54	**0.48**
	25s	7.91	7.97	7.97	**0.41**
	27s	0.28	0.29	0.29	**0.27**
	32s	0.32	0.33	0.33	**0.25**
	37s	0.37	0.38	0.38	**0.35**
	38s	0.4	0.41	0.41	**0.35**
	43s	2.11	2.14	2.14	**0.58**
	44s	0.28	0.29	0.29	**0.26**
	46s	0.88	0.89	0.89	**0.29**
	49s	2.83	2.84	2.84	**0.44**
DLX processor	dlx1c	3.16	3.54	3.34	**0.36**
	dlx1c.rwmem	4	4.95	4.86	**0.41**
	dlx1c.rwmem1	4.18	4.57	4.55	**0.39**
Elf processor	6steps	0.09	**0.1**	**0.1**	0.21
	7steps	0.43	0.44	0.44	**0.31**
	8steps	2.49	2.52	2.53	**0.5**
	9steps	15.67	16.21	16.3	**1.26**
	10steps	7.38	24.18	21.57	**6.11**
	12steps	21.13	2436	1612	**567**
Out of order processor (rf)	6steps	0.56	0.57	0.57	**0.28**
	7steps	1.23	1.28	1.28	**0.4**
	8steps	2.24	2.55	2.59	**0.96**
	9steps	3.83	5.76	5.73	**2.8**
	10steps	5.88	42.63	58.62	**16.81**
	11steps	8.83	2403	1111	**92**
	12steps	12.75	+6000	+6000	**859**
	13steps	17.65	+6000	+6000	**5413**
Out of order processor (tag)	8steps	1.16	1.2	1.2	**0.44**
	10steps	3.47	4.18	4.54	**0.93**
	12steps	8.19	12.96	11.44	**3**
	14steps	16.56	31.08	38.18	**13.68**
	15steps	22.71	47.67	**45.55**	51.89
	17steps	34.3	1959	1499	**201**
	19steps	54.47	+6000	+6000	**1709**
Load-Store processor	6steps	0.19	0.2	0.2	**0.06**
	8steps	1.08	1.12	1.12	**0.41**
	10steps	4.77	4.99	4.95	**1.2**
	12steps	21.48	23.69	23.69	**4.16**
	14steps	12.58	**15.33**	15.42	24.43
Cache Coherence Protocol	8steps	0.78	0.79	0.79	**0.61**
	10steps	1.37	**1.38**	**1.38**	4.29
	12steps	2.51	2.62	**2.58**	26.33
	14steps	4.07	**5.24**	5.78	83.72
	15steps	5.07	**8.08**	10.27	163
	16 steps	6.4	22	**21**	377
	17 steps	7.75	48.08	**45.64**	794
	18 steps	9.39	**110.25**	140.7	2115
Two queues	10steps	0.44	0.5	0.53	**0.25**
	12steps	0.68	0.98	1.06	**0.4**
	14steps	0.93	6.41	5.73	**0.95**
	18steps	1.61	432	802	**14**
	20steps	2.08	+6000	+6000	**58**

SUMMARY OF RESULTS (Siege)

SD

Family	**Siege_v3**	**Siege_v4**	**DPLL(T)**
Buggy Cache Coherence	**2.35**	2.57	6.66
Code Validation Suite	34.49	33.76	**3.68**
DLX processor	11.63	11.67	**1.16**
Elf processor	4987	3585	**575**
Out of order processor (rf)	18839 (3 TO)	18689 (3 TO)	**6385**
Out of order processor (tag)	**188**	210.6	1979
Load-Store processor	55.72	54.44	**30.26**
Cache Coherence Protocol	5517	4594	**3601**
Two queues	1529	858	**73.6**

EIJ

Family	**Siege_v3**	**Siege_v4**	**DPLL(T)**
Buggy Cache Coherence	7.17	**6.37**	6.66
Code Validation Suite	41.05	40.93	**3.68**
DLX processor	13.74	13.98	**1.16**
Elf processor	12021 (2 MO)	12021 (2 MO)	**575**
Out of order processor (rf)	12420 (2 TO)	12292 (2 TO)	**6385**
Out of order processor (tag)	**400**	749	1979
Load-Store processor	6035 (1 MO)	6035 (1 MO)	**30.26**
Cache Coherence Protocol	18309 (3 MO)	18228(3 MO)	**3601**
Two queues	18033 (3 MO)	18031 (3 MO)	**73.6**

Hybrid 1

Family	**Siege_v3**	**Siege_v4**	**DPLL(T)**
Buggy Cache Coherence	**6.33**	7.24	6.66
Code Validation Suite	13.41	13.41	**3.68**
DLX processor	13.75	13.96	**1.16**
Elf processor	1060	6045 (1 TO)	**575**
Out of order processor (rf)	12407 (2 TO)	12303 (2 TO)	**6385**
Out of order processor (tag)	431	**409**	1979
Load-Store processor	73.61	79.45	**30.26**
Cache Coherence Protocol	18235 (3 MO)	18230 (3 MO)	**3601**
Two queues	18031 (3 MO)	18033 (3 MO)	**73.6**

Hybrid 2

Family	**Siege_v3**	**Siege_v4**	**DPLL(T)**
Buggy Cache Coherence	**3.16**	3.66	6.66
Code Validation Suite	28.09	28.08	**3.68**
DLX processor	13.06	12.75	**1.16**
Elf processor	2479	1653	**575**
Out of order processor (rf)	14456 (2 TO)	13180 (2 TO)	**6385**
Out of order processor (tag)	8056 (1 TO)	7600 (1 TO)	**1979**
Load-Store processor	45.33	45.38	**30.26**
Cache Coherence Protocol	**198**	228	3601
Two queues	6440 (1 TO)	6809 (1 TO)	**73.6**

TO: time out
MO: memory out

Family	File	SVC	ICS	DPLL(T)
Buggy Cache Coherence	Bug1	+6000	169	**5.98**
	Bug2	**0.4**	10.4	0.67
Code Validation Suite	22s	9.52	0.74	**0.48**
	25s	13.54	**0.41**	**0.41**
	27s	**0.05**	0.1	0.27
	32s	**0.04**	0.07	0.25
	37s	**0.14**	0.22	0.35
	38s	**0.12**	0.35	0.35
	43s	32.59	52.36	**0.58**
	44s	**0.07**	0.18	0.26
	46s	**0.12**	0.18	0.29
	49s	0.67	**0.06**	0.44
DLX processor	dlx1c	5.62	0.93	**0.36**
	dlx1c.rwmem	5.62	1.24	**0.41**
	dlx1c.rwmem1	5.71	1.34	**0.39**
Elf processor	6steps	**0.01**	**0.01**	0.21
	7steps	**0.19**	0.22	0.31
	8steps	0.74	bug	**0.5**
	9steps	5.06	bug	**1.26**
	10steps	71.98	bug	**6.11**
	12steps	+6000	+6000	**567**
Out of order processor (rf)	6steps	0.14	**0.11**	0.28
	7steps	0.63	0.47	**0.4**
	8steps	3.18	1.8	**0.96**
	9steps	17	9.37	**2.8**
	10steps	94.62	58.13	**16.81**
	11steps	550	388	**92**
	12steps	+6000	memory	**859**
	13steps	+6000	memory	**5413**
Out of order processor (tag)	8steps	3.3	0.45	**0.44**
	10steps	118	3.27	**0.93**
	12steps	4667	46.11	**3**
	14steps	+6000	memory	**12.52**
	15steps	+6000	memory	**51.89**
	17steps	+6000	+6000	**201**
	19steps	+6000	+6000	**1709**
Load-Store processor	6steps	2.7	0.09	**0.06**
	8steps	473	1.01	**0.41**
	10steps	+6000	166	**1.2**
	12steps	+6000	+6000	**4.16**
	14steps	+6000	memory	**24.43**
Cache Coherence Protocol	8steps	**0.34**	7.6	0.61
	10steps	**3.12**	101	4.29
	12steps	63.83	1913	**26.33**
	14steps	2045	+6000	**83.72**
	15steps	+6000	+6000	**163**
	16steps	+6000	+6000	**377**
	17steps	+6000	+6000	**794**
	18steps	+6000	+6000	**2152**
Two queues	10steps	0.7	4.76	**0.25**
	12steps	3.34	26.18	**0.4**
	14steps	15.68	144	**0.95**
	18steps	335	memory	**14**
	20steps	1517	memory	**58**

CONCLUSION

As expected, translation-based methods will normally outperform DPLL(T) for problems where the theory T plays a very small role. But this is no longer the case when theory predicates start playing a significant role, as in the families Code Validation, Elf and OOO processors (rf), and Two queues. To illustrate this phenomenon with an extreme case, we have also run experiments from finite group theory. For example, the 4-S formula says that groups of cardinality 4 exist, i.e., that the elements (represented by constants a, b, c, d) are pairwise distinct, all instances with a, b, c, d of the group axioms hold ($f(e, a) = a$, $f(e, b) = b$, etc.), and the operations are closed ($i(a)$=$a \vee i(a)$=$b \vee i(a)$=$c \vee i(a)$=d, etc.). The experiments are summarized in the table below reporting BerkMin's run times for each translation-based approach (with translation times in parentheses), together with SVC's and DPLL(T)'s run times.

Groups										
steps	**SD**		**EIJ**		**Hyb1**		**Hyb2**		**SVC**	**DPLL(T)**
3-S	8.06	(7.48)	492	(490)	492	(489)	7.5	(6.9)	**0.1**	**0.1**
3-US	27.3	(7.7)	494	(489)	493	(7.7)	26.8	(62)	**0.2**	**0.2**
4-S	54.7	(50.7)		(1m)		(1m)	51.2	(47.4)	**0.2**	**0.2**
4-US	711	(50.9)		(1m)		(1m)	710	(48.2)	**0.2**	**0.2**

As for how our tool compares with the lazy approach of ICS or SVC, these experiments show that DPLL(T) clearly outperforms their approach at least for the set of benchmarks we have used. Only future work will answer whether this behaviour will extend to some richer logics.