

Curriculum Vitæ

Jordi Cortadella

December 11, 2011

Summary

Jordi Cortadella is a full professor at the Department of Software of the *Universitat Politècnica de Catalunya* (Barcelona, Spain). He obtained his Ph.D. in Computer Science in 1987, at the same University. In 1988, he was a Visiting Scholar at the University of California, Berkeley. He has also been a visiting professor in Intel Corporation (Hillsboro, USA) in summer 1998 and summer 2001 and in Theseus Logic (Sunnyvale, USA) in summer 2000. He co-founded Elastix Corporation in 2007, a company producing EDA tools for asynchronous design.

His main research interests include formal methods and computer-aided design of VLSI systems, with special emphasis on asynchronous circuits. He has co-authored over 150 papers in technical journals and conferences. He has served in the technical programme committee of numerous conferences in the area of computer-aided design of VLSI systems and concurrency.

His research has had a relevant impact in the scientific community. As an example, he designed an arithmetic circuit for fast addition and comparison, published in 1992. This circuit drew the attention of the designers of the IBM high-speed microprocessor *guTS*, and was incorporated in the integer arithmetic unit (see Hofstee et al., *Designing for a gigahertz*, IEEE Micro, Vol. 18, No. 3, May/June 1998). The designers of the UltraSPARC stations, from Sun Microsystems, also used the same circuit in the memory system (see Heald et al., *64-KByte sum-addressed-memory cache with 1.6-ns cycle and 2.6-ns latency*, IEEE Journal of Solid-State Circuits, Vol. 33, No. 11, Nov. 1998).

His contributions in the area of the synthesis and analysis of concurrent systems have also had a tangible impact. One of his most referenced papers is *Petri net analysis using Boolean manipulation* (Lecture Notes in Computer Science 815, June 1994), co-authored with E. Pastor, O. Roig and R.M. Badia.

However, the most relevant work has been in the area of asynchronous circuits. He has been working on this subject during more than 15 years, in a tight collaboration with an international team: Dr. M. Kishinevsky (Intel Corp., USA), Dr. A. Kondratyev (Cadence Design Systems, USA), Prof. L. Lavagno (Politecnico di Torino, Italy) and Prof. A. Yakovlev (University of Newcastle upon Tyne, UK). The activities in this area can be qualified as *basic research*, but the obtained results have raised the interest of many industrial and academic institutions. The most observable results of this research, a tool for the synthesis of asynchronous controllers called *petrify* (www.lsi.upc.es/petrify) is currently being used by many Universities for research and teaching activities: University of Manchester (UK), Technion (Israel), Boston University (USA), McGill University (Canada), IIT Bombay (India), KAIST (Korea), University of Augsburg (Germany), Technical University of Denmark, CSEM (Switzerland), etc. Some industries are also using the tool for their internal research: Intel Corporation (USA), Theseus Logic (USA) and Cadence Design Systems (USA). This impact is also manifested by a frequently cited paper in this area: *Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers*, IEICE Trans. on Information and Systems, March 1997.

He has published numerous papers in international journals: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *Proceedings of the IEEE*, *IEEE Transactions on Computers*, *IEEE Transactions on VLSI*, etc. Most of the contributions in this area have been covered by the book

J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev,
Logic synthesis of asynchronous controllers and interfaces,
Springer Verlag, 2002.

The impact of his research has also been recognized by the nomination as a finalist of the *Descartes Prize 2002* and three best paper awards at the *Design Automation Conference* (2004), *Int. Symp. on Advanced Research in Asynchronous Circuits and Systems* (2004) and *Int. Conf. on Application of Concurrency to System Design* (2009). He also obtained a *Distinction* for the Promotion of the University Research by the Generalitat de Catalunya in 2003.

The relevance of his work has also been recognized by the invitation to give tutorials and talks in prestigious conferences. As an example, only in the area of design of asynchronous circuits, Jordi Cortadella has given tutorials in Grenoble (Summer School, 2002), India (VLSI Design Conference, 2002), Aarhus (Conference on Petri Nets 2000), Israel (Conference on Asynchronous Circuits, 2000), among many others.

Besides the public funding obtained from National and European Projects, Jordi Cortadella has also been involved in technology transfer actions to important companies in the microelectronics area from United States: Intel Corporation, Cadence Design Systems and Theseus Logic.

Finally, research has been time-shared with several academic positions involving different management activities in the University: Vicedean of the *Facultat d'Informàtica de Barcelona*, President of the Comission for the Evaluation and Selection of Academic Staff of the UPC, Member of the Comission of Ph.D. programs of the UPC, Coordinator of two Ph.D. programs (Computer Architecture and Software), etc.

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1 Personal data

Name: Jordi Cortadella Fortuny

Birthdate and birthplace: January 29th, 1962. Martorell, Spain.

University: Universitat Politècnica de Catalunya.

Departament: Llenguatges i Sistemes Informàtics.

Position: Catedràtic d'Universitat (Full professor).

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2 Academic degrees

- *Llicenciat en Informàtica* (B.S. in Computer Science),
Facultat d'Informàtica de Barcelona (UPC). June 1985.
- *Llicenciat amb grau en Informàtica* (M.S. in Computer Science)
Facultat d'Informàtica de Barcelona (UPC). February 1986.
Qualification: Matrícula de Honor.
- *Doctor en Informàtica*, (Ph.D. in Computer Science)
Facultat d'Informàtica de Barcelona (UPC). June 1987.
Qualification: Apto "Cum Laude" by unanimity.

3 Awards

- Best paper award at the *Int. Conference on Application of Concurrency to System Design (ACSD)*, for the paper *Scheduling synchronous elastic designs*. June 2009.
- Best paper award at the *Design Automation Conference*, for the paper *A Recursive Paradigm to Solve Boolean Relations*. June 2004.
- Best paper award at the *Int. Symp. on Advanced Research in Asynchronous Circuits and Systems*, for the paper *Handshake protocols for de-synchronization*. April 2004.
- Distinction for the Promotion of University Research, by the Generalitat de Catalunya (Distinció de la Generalitat per a la Promoció de la Recerca Universitària), 2003.
- Finalist of the *Descartes prize 2002*, with the project *Petrify: methodology and tool for logic synthesis of asynchronous circuits*. Coordinator of the project (see www.cordis.lu/descartes).
- Best Ph.D. thesis award, Universitat Politècnica de Catalunya, 1992.
- National Award for the best student in Computer Science, 1986. (1er. premio nacional de Terminación de Estudios en Informática).

4 Positions

4.1 Academic positions

<u>Period</u>	<u>Position</u>	<u>Department</u>
Oct. 1985 - May 1988	Assistant Professor	Computer Architecture (UPC)
June 1988 - June 1997	Associate Professor	Computer Architecture (UPC)
July 1997 - Oct. 1999	Associate Professor	Software (UPC)
since Nov. 1999	Full Professor	Software (UPC)

4.2 Industrial positions

In June 2007, Jordi Cortadella co-founded Elastix Corporation, with Vigyan Singhal and Emre Tuncer. Elastix Corporation is a company devoted to the design of energy-efficient circuits using de-synchronization.

4.3 Visiting positions

July 1988 – December 1988: Visiting professor at the Electrical Engineering and Computer Science Department at the University of California, Berkeley.

July 1998 – September 1998: Visiting professor at the Strategic CAD Labs, Intel Corporation, Hillsboro, OR.

July 2000 – September 2000: Visiting professor at Theseus Logic Sunnyvale, CA.

July 2001 – September 2001: Visiting professor at the Strategic CAD Labs, Intel Corporation, Hillsboro, OR.

5 Thesis advisor

5.1 Ph.D. thesis advisor

- Marc Galceran-Oms,
Automatic Pipelining of Elastic Systems,
Universitat Politècnica de Catalunya, September 2011. Co-advised with Mike Kishinevsky.
- Kyller Costa Gorgônio,
Towards the Automatic Synthesis of Asynchronous Communication Mechanisms,
Universitat Politècnica de Catalunya, December 2010.
- Dmitry Bufistov,
Performance Optimization of Elastic Systems,
Universitat Politècnica de Catalunya, December 2010.
- David Bañeres,
Logic Synthesis Techniques for High-Speed Circuits,
Universitat Politècnica de Catalunya, February 2008. Co-advised with Mike Kishinevsky.
- Robert Clarisó,
Abstract Interpretation Techniques for the Verification of Timed Systems,
Universitat Politècnica de Catalunya, September 2005.
- Josep Carmona,
Structural Methods for the Synthesis of Well-Formed Concurrent Specifications,
Universitat Politècnica de Catalunya, March 2004.

- Marco A. Peña,
Relative Timing Based Verification of Concurrent Systems,
Universitat Politècnica de Catalunya, April 2003. Co-advised with Enric Pastor.
- Gianluca Cornetta,
Design and Analysis of Variable-Delay Arithmetic Units,
Universitat Politècnica de Catalunya, December 2001.
- Oriol Roig Mansilla,
Formal Verification and Testing of Asynchronous Circuits,
Universitat Politècnica de Catalunya, May 1997.
- Enric Musoll Cinca,
High-level and logic synthesis techniques for low power,
Universitat Politècnica de Catalunya, July 1996.
- Enric Pastor Llorens,
Structural Methods for the Synthesis of Asynchronous Circuits from Signal Transition Graphs,
Universitat Politècnica de Catalunya, April 1996.
- Fermín Sánchez Carracedo,
Loop pipelining with resource and timing constraints,
Universitat Politècnica de Catalunya, January 1996.
- Rosa M. Badia Sala,
High-level synthesis of asynchronous circuits,
Universitat Politècnica de Catalunya, July 1994.
- Teodor Jové Lagunas,
Design of instruction memories for pipelined processors,
Universitat Politècnica de Catalunya, October 1989.

5.2 Master thesis advisor

- Andrey Ziyatdinov, *Multi-Clustering net Model for VLSI Placement*, September 2008.
- Jonas Casanova Bachs, *Clustering for the optimization of asynchronous controllers*, June 2008.
- Dmitry Bufistov, *Performance optimization of latency insensitive systems*, February 2008.
- Marc Galceran Oms, *Elastic Esterel*, July 2007.

6 Funded research projects

6.1 Grants from Industry

- *Methodology and tools for the specification, synthesis and verification of asynchronous circuits with relative timing*,
funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 1999-2002. Principal investigator.
- *Design automation for embedded electronic systems*,
funded by Cadence Design Systems (Cadence Berkeley Labs, Berkeley, USA), 2001-2003. Principal investigator.
- *Reencoding Techniques for Logic Synthesis of High-speed Circuits*,
funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2002-2004. Principal investigator.

- *Design, synthesis and evaluation of elastic architectures*, funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2005-2007. Principal investigator.
- *Collaboration agreement between Elastix Corporation and Universitat Politècnica de Catalunya* for research on asynchronous circuits. Since 2007.
- *Synthesis of scalable systems for nanoelectronics*, funded by Intel Corporation (Strategic CAD Lab, Hillsboro, OR(USA)), 2008-2009. Principal investigator.

6.2 European projects

- *ATD: Technology for ATD* (RACE 1022), 1990–1992. Investigator (principal investigator: Mateo Valero).
- *ACiD-WG: Asynchronous Circuit Design* (ESPRIT-7225), 1992-1995. Principal investigator at UPC.
- *SHIPS: Supercomputer Highly Parallel System* (ESPRIT-6253), 1992-1995. Investigator (principal investigator: Mateo Valero).
- *ACiD-WG: Asynchronous Circuit Design* (ESPRIT-21949), 1996-2000. Principal investigator at UPC.
- *COSY: COdesign, Simulation & sYnthesis* (ESPRIT EP 25443), 1997-2000. Principal investigator at UPC.
- *ACiD-WG: Asynchronous Circuit Design* (IST-1999-21949), 2000-2004. Principal investigator at UPC.
- *SegraVIS: Syntactic and Semantic Integration of Visual Modelling Techniques* (RTN2-2001-00346), 2002-2005. Investigator (principal investigator at UPC: Fernando Orejas).

6.3 CICYT projects (Spanish Comission for Science and Technology)

- *Design of high-performance low-cost parallel architectures*, 1986-1989, investigator (principal investigator: Mateo Valero).
- *VLSI architectures oriented to high-level languages*, 1989—1991, principal investigator.
- *Parallel architectures oriented to symbolic applications*, 1991–1994, principal investigator.
- *Design and verification of low-power, high-performance circuits*, 1994–1995, principal investigator.
- *Application-specific high-speed low-power architectures*, 1995–1998, principal investigator.
- *Codesign of heterogeneous concurrent systems*, 1999–2001, principal investigator.
- *Heterogeneity and Modularity in the Specification of Systems*, 1999–2001, investigator (principal investigator: Fernando Orejas).
- *Modelling, Analysis and Verification of Heterogeneous Systems*, 2002-2004, investigator (principal investigator: Fernando Orejas).
- *Graph-based methods for the modelling, analysis and implementation of large-scale systems*, 2005-2007, investigator (principal investigator: Fernando Orejas).
- *Formal methods and algorithms for system design*, 2007-2012, investigator (principal investigator: Fernando Orejas).

6.4 Integrated actions

- *CAD tools for the synthesis of asynchronous digital circuits*, Integrated action Spain-UK with the University of Newcastle upon Tyne, 1996-97, principal investigator at UPC.
- *Modelling and synthesis of asynchronous arbiters*, Integrated action Spain-Portugal with the University of Aveiro, 1996-97, principal investigator at UPC.
- *CAD tools for the synthesis of asynchronous digital circuits with bounded delays*, Integrated action Spain-UK with the University of Newcastle upon Tyne, 1998-99, principal investigator at UPC.

7 Technology transfer

7.1 Elastix Corporation

In 2007, he co-founded Elastix Corporation, a company aiming at the design of energy-efficient systems using asynchronous circuits.

7.2 Petrify

Petrify is a tool for the synthesis of Petri nets and asynchronous circuits (50,000 lines of C code approximately). The theoretical background of the tool has been a joint work with Dr. M. Kishinevsky (Intel Corp.), A. Kondratyev (Cadence Berkeley Labs), L. Lavagno (Politecnico di Torino), A. Yakovlev (University of Newcastle upon Tyne). This background has been published in numerous journal and conference papers and collected in a book:

J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno and A. Yakovlev,
Logic Synthesis of Asynchronous Controllers and Interfaces,
Springer-Verlag, 2002.

Petrify (<http://www.lsi.upc.es/petrify>) is a public domain tool currently being used by more than 20 academic and industrial institutions: Intel Corp., Theseus Logic, Manchester University (UK), Technical University of Denmark, Technion (Israel), AT&T Labs (Cambridge, UK), University of North Carolina at Chapel Hill (USA), etc. *Petrify* has also been integrated with synthesis flow of Theseus Logic (Sunnyvale, USA) and the logic synthesis system SIS from UC Berkeley.

7.3 Police Criterion Chip

Design and implementation of the *Police Criterion Chip*, an integrated circuit for traffic control in broadband communication network (300.000 transistors, CMOS technology). This prototype was developed within the project RACE 1022 “*Technology for ATD*”. It was a joint work with Anna del Corral and Eduard Elias (from the Computer Architecture Department).

8 Patents

- *Skew insensitive clocking method and apparatus*,
Patent Number: 7,634,749,
Inventors: Jordi Cortadella, Alex Kondratyev and Luciano Lavagno,
Assignee: Cadence Design Systems, Inc.,
Issued on: Dec 15, 2009.
- *Synchronous elastic designs with early evaluation*,
Patent Number: 7,657,862,

Inventors: Mike Kishinevsky and Jordi Cortadella,
Assignee: Intel Corporation,
Issued on: Feb 2, 2010.

- *Variability-aware scheme for asynchronous circuit initialization*,
Patent Number: 7,701,255,
Inventors: Jordi Cortadella, Vigyan Singhal and Emre Tuncer,
Assignee: Elastix Corporation,
Issued on: April 20, 2010.

9 Academic activities

9.1 Organization and participation in scientific events

Organization of events:

- *16th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'09)*, Grenoble, May 2010. Best Paper Chair.
- *14th International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'08)*, Newcastle, April 2008. Program co-chair.
- *International Conference on Application and Theory of Petri Nets (ICATPN)*. Program co-chair, 2004.
- *Workshop on Token-Based Computing (ToBaCo)*. Workshop co-organizer, Bologna, June 2004.
- *European Joint Conferences on Theory and Practice of Software (ETAPS)*. Workshop Chair, 2004.
- *Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC'99)*, Barcelona, April 1999. General chair.
- *Hawaii International Conference on System Sciences*. Hawaii, January 1994. Co-organizer of the mini-track *Design and Prototyping of Digital Signal Processing Systems*.
- *EUROMICRO'93*. Barcelona, September 1993. Conference co-organizer.
- *ACiD-WG Workshop on Digital Signal Processing*. Barcelona, September 1993. Workshop organizer.

Member of Program Committees:

- *Conference on Design, Automation and Test in Europe (DATE)* (1998, 2002, 2006, 2007).
- *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)* (1997, 1998, 2003).
- *ACM/IEEE Design Automation Conference (DAC)* (2007).
- *International Symposium on Advanced Research in Asynchronous Circuits and Systems (ASYNC)* (1996–2000, 2002–2003).
- *International Conference on Application and Theory of Petri Nets (ICATPN)* (2001–2003).
- *International Conference on Application of Concurrency to System Design (ACSD)* (1998, 2003).
- *Symposium in Computer Arithmetic* (1997)
- *Joint Conference on Formal Modelling and Analysis of Timed Systems (FORMATS) and Formal Techniques in Real-Time and Fault Tolerant Systems (FTRTFT)* (2004).
- *International Workshop on Formal Modeling and Analysis of Timed Systems (FORMATS)* (2003).
- *Symposium on Integrated Circuits and Systems Design (SBCCI)* (2003).
- *Asian South Pacific Design Automation Conference (ASP-DAC)* (2003).
- *International Symposium on System Synthesis (ISSS)* (2000).

- *IEEE/ACM International Workshop on Logic Synthesis (IWLS)* (1998–2000, 2002, 2003, 2004).
- *Conference in Design of Integrated Circuits and Systems (DCIS)* (1996).
- *Second Working Conference on Asynchronous Design Methodologies* (1995).
- *International Symposium on Microprocessing and Microprogramming (EUROMICRO)* (1990–1994).
- *Conference on Simulation in Electronics* (1994).

Journals:

- Guest Editor of the *IEEE Transactions on VLSI Systems Special Section on Asynchronous Circuits and Systems*, 2008.
- Reviewer for the following journals:
 - *ACM Transactions on Design Automation of Electronic Systems*.
 - *IEEE Transactions on Computers*.
 - *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
 - *IEEE Transactions on VLSI Systems*.
 - *IEEE Transactions on Circuits and Systems*.
 - *IEEE Transactions on Parallel and Distributed Systems*.
 - *Distributed Computing*.
 - *Formal Methods in Systems Design*.
 - *Formal Aspects of Computing: The International Journal of Formal Methods*.
 - *Fundamenta Informaticae*.
 - *Integration: The VLSI journal*.
 - *Journal of VLSI-Signal Processing*.
 - *IEE Proceedings: Computers and Digital Techniques*.
 - *Journal on Microprocessing and Microprogramming*.

9.2 Positions at the University

9.2.1 Universitat Politècnica de Catalunya

- Member of the Commission of Ph.D. programs, June 1996 - June 2000.
- Member and president of the Commission for the Evaluation and Selection of Academic Staff (CSAPIU), since Nov. 2000 - Dec 2003.

9.2.2 Facultat d’Informàtica de Barcelona (UPC)

- *Vicedean of Resources*, Mar. 1990 - Sept. 1991.
- Member of the Commission for the elaboration of the new Studies Plan, Sept. 1990 - June 1991.
- Member of the Permanent Commission, Mar. 1990 - Dec. 1992 and Dec. 1993 - Dec. 1996.
- Member of the Academic Commission (Comissió Docent), academic years 1989-90 and 1991-92.
- Member of the “Junta de Facultat”, Oct. 1985 - Oct. 1997 and Dec. 1999 - dec. 2001.
- Member of the Commission of the CS Library (Oct. 1995 - July 2000).

9.2.3 Departament of Software (UPC)

- Coordinator of the Ph.D. program in Software, Dec. 1999 - Dec. 2002.
- Member of the “Junta de Departament”, Feb. 2000 - Feb. 2002.
- President of the Commission of Postgraduate Studies, Oct 2005 - June 2007.
- Subdirector of Department, Oct 2005 - Dec 2009.

9.2.4 Departament of Computer Architecture (UPC)

- Member of the Commission for graduate studies, Oct. 1990 - May. 1994.
- Member of the Commission for Research Evaluation, Mar.1993 - Apr. 1995.
- Member of the Commission for the evaluation of teaching activities, Oct. 1992 - Feb. 1993.
- Coordinator of undergraduate studies, Mar. 1989 - Feb. 1990.
- Member of the “Junta de Departament”, Jan. 1990 - Feb. 1993.
- Coordinator of the Ph.D. program in “Computer Architecture and Technology”, Apr. 1995 - May 1997.

10 Publications

10.1 Books and book chapters

- [1] Jordi Cortadella and Wolfgang Reisig, editors. *Applications and Theory of Petri Nets 2004*, volume 3099 of *Lecture Notes in Computer Science*. Springer-Verlag, 2004.
- [2] Josep Carmona, Jordi Cortadella, Victor Khomenko, and Alex Yakovlev. Synthesis of asynchronous hardware from Petri nets. In J. Desel, W. Reisig, and G. Rozenberg, editors, *Lectures on Concurrency and Petri Nets: Advances in Petri Nets*, volume 3098 of *Lecture Notes in Computer Science*, pages 345–401. Springer-Verlag, 2004.
- [3] Jordi Cortadella, Alexandre Yakovlev, and Grzegorz Rozenberg, editors. *Advances in Concurrency and Hardware Design*, volume 2549 of *Lecture Notes in Computer Science*. Springer-Verlag, November 2002.
- [4] Josep Carmona, Jordi Cortadella, and Enric Pastor. Synthesis of reactive systems: Application to asynchronous circuit design. In J. Cortadella, A. Yakovlev, and G. Rozenberg, editors, *Advances in Concurrency and Hardware Design*, volume 2549 of *Lecture Notes in Computer Science*, pages 108–151. Springer-Verlag, 2002.
- [5] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. *Logic synthesis of asynchronous controllers and interfaces*. Advanced Microelectronics. Springer-Verlag, 2002.
- [6] Fermín Sánchez and Jordi Cortadella. Resource-constrained software pipelining for high-level synthesis of dsp systems. In M. Moonen and F. Catthoor, editors, *Algorithms and Parallel VLSI Architectures III*. Elsevier Science Publishers, 1995.
- [7] Jordi Cortadella, José M. Llabería, and Mateo Valero. Arquitecturas orientadas a lenguajes basados en la lógica. In *Inteligencia Artificial*, chapter 21, pages 233–243. Ed. Marcombo, 1987.
- [8] Jordi Cortadella. *Mechanisms for the efficient execution of branches in RISC architecture*. PhD thesis, Universitat Politècnica de Catalunya, 1987. (In Spanish).

10.2 Journals

- [1] Marc Galceran-Oms, Alexander Gotmanov, Jordi Cortadella, and Mike Kishinevsky. Microarchitectural transformations using elasticity. *7:18:1–18:24*, December 2011.
- [2] Josep Carmona, Jorge Júlvez, Jordi Cortadella, and Michael Kishinevsky. A scheduling strategy for synchronous elastic designs. *Fundamenta Informaticae*, 108(1-2):1–21, 2011.
- [3] Josep Carmona, Jordi Cortadella, Mike Kishinevsky, and Alexander Taubin. Elastic circuits. *IEEE Transactions on Computer-Aided Design*, 28(10):1437–1455, October 2009.
- [4] Josep Carmona, Jordi Cortadella, and Mike Kishinevsky. New region-based algorithms for deriving bounded Petri nets. *IEEE Transactions on Computers*, 59(3):371–384, March 2010.
- [5] Jordi Cortadella and Alexander Taubin. Guest editorial: Special section on asynchronous circuits and systems. *IEEE Transactions on VLSI Systems*, 17(7):853–854, July 2009.
- [6] Jorge Júlvez, Jordi Cortadella, and Michael Kishinevsky. On the performance evaluation of multi-guarded marked graphs with single-server semantics. *Discrete Event Dynamic Systems*, 20(3):377–407, September 2010.
- [7] Jordi Cortadella, Michael Kishinevsky, Dmitry Bufistov, Josep Carmona, and Jorge Júlvez. Elasticity and Petri Nets. *Transactions on Petri Nets and Other Models of Concurrency I*, 5100:221–249, August 2008.
- [8] David Bañeres, Jordi Cortadella, and Mike Kishinevsky. A recursive paradigm to solve Boolean relations. *IEEE Transactions on Computers*, 58(4):512–527, April 2009.
- [9] Josep Carmona, Jordi Cortadella, Yousuke Takada, and Ferdinand Peper. Formal methods for the analysis and synthesis of nanometer-scale cellular arrays. *ACM Journal on Emerging Technologies in Computing Systems*, 4(2), 2008.
- [10] Josep Carmona and Jordi Cortadella. Encoding large asynchronous controllers with ILP techniques. *IEEE Transactions on Computer-Aided Design*, 27(1):20–33, January 2008.
- [11] Alexander Taubin, Jordi Cortadella, Luciano Lavagno, Alex Kondratyev, and Ad Peeters. Design automation of real life asynchronous devices and systems. *Foundations and Trends in Electronic Design Automation*, 2(1):1–133, 2007.
- [12] Robert Clarisó and Jordi Cortadella. Verification of concurrent systems with parametric delays using octahedra. *Fundamenta Informaticae*, 78(1):1–33, 2007.
- [13] Kyller Costa Gorgônio, Jordi Cortadella, Fei Xia, and Alexandre Yakovlev. Automating synthesis of asynchronous communication mechanisms. *Fundamenta Informaticae*, 78(1):75–100, 2007.
- [14] Robert Clarisó and Jordi Cortadella. The octahedron abstract domain. *Science of Computer Programming*, 64(1):115–139, January 2007.
- [15] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, and Christos Sotiriou. Desynchronization: Synthesis of asynchronous circuits from synchronous specifications. *IEEE Transactions on Computer-Aided Design*, 25(10):1904–1921, October 2006.
- [16] Josep Carmona, José M. Colom, Jordi Cortadella, and Fernando García-Vallés. Synthesis of asynchronous controllers using integer linear programming. *IEEE Transactions on Computer-Aided Design*, 25(9):1637–1651, September 2006.
- [17] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Claudio Passerone, and Yosinori Watanabe. Quasi-static scheduling of independent tasks for reactive systems. *IEEE Transactions on Computer-Aided Design*, 24(10):1492–1514, October 2005.

- [18] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Alexander Taubin, and Yosinori Watanabe. Quasi-static scheduling for concurrent architectures. *Fundamenta Informaticae*, 62(2):171–196, July 2004.
- [19] Jordi Cortadella. Timing-driven logic bi-decomposition. *IEEE Transactions on Computer-Aided Design*, 22(6):675–685, June 2003.
- [20] Hiroshi Saito, Alex Kondratyev, Jordi Cortadella, Luciano Lavagno, Takashi Nanya, and Alexander Yakovlev. Design of asynchronous controllers with delay insensitive interface. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, E85-A(12):2577–2585, December 2002.
- [21] Josep Carmona, Jordi Cortadella, and Enric Pastor. A structural encoding technique for the synthesis of asynchronous circuits. *Fundamenta Informaticae*, 50(2):135–154, March 2002.
- [22] Jordi Cortadella, Michael Kishinevsky, Steve M. Burns, Alex Kondratyev, Luciano Lavagno, Ken S. Stevens, Alexander Taubin, and Alexandre Yakovlev. Lazy transition systems and asynchronous circuit synthesis with relative timing assumptions. *IEEE Transactions on Computer-Aided Design*, 21(2):109–130, February 2002.
- [23] Enric Pastor, Jordi Cortadella, and Oriol Roig. Symbolic analysis of bounded Petri nets. *IEEE Transactions on Computers*, 50(5):432–448, May 2001.
- [24] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, Enric Pastor, and Alexandre Yakovlev. Decomposition and technology mapping of speed-independent circuits using Boolean relations. *IEEE Transactions on Computer-Aided Design*, 18(9):1221–1236, September 1999.
- [25] Fermín Sánchez and Jordi Cortadella. Optimal exploration of the unrolling degree for software pipelining. *Journal of Systems Architecture*, 45(6–7):505–517, 1999.
- [26] Alex Kondratyev, Jordi Cortadella, Michael Kishinevsky, Luciano Lavagno, and Alexander Yakovlev. Logic decomposition of speed-independent circuits. *Proceedings of the IEEE*, 87(2):347–362, February 1999.
- [27] Enric Musoll, Tomás Lang, and Jordi Cortadella. Working-zone encoding for reducing the energy in microprocessor address buses. *IEEE Transactions on VLSI Systems*, 6(4):568–572, December 1998.
- [28] Enric Pastor, Jordi Cortadella, Alex Kondratyev, and Oriol Roig. Structural methods for the synthesis of speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, 17(11):1108–1129, November 1998.
- [29] Jordi Cortadella, Michael Kishinevsky, Luciano Lavagno, and Alexandre Yakovlev. Deriving Petri nets from finite transition systems. *IEEE Transactions on Computers*, 47(8):859–882, August 1998.
- [30] Enric Musoll and Jordi Cortadella. Register-transfer level transformations for low-power data-paths. *Integrated Computer-Aided Engineering*, 5(4):315–332, 1998.
- [31] Fermín Sánchez and Jordi Cortadella. Reducing register pressure in software pipelining. *Journal of Information Science and Engineering (special issue on Compiler Techniques for High-Performance Computing)*, 14(1):265–279, March 1998.
- [32] A. Kondratyev, M. Kishinevsky, A. Taubin, J. Cortadella, and L. Lavagno. The use of Petri nets for the design and verification of asynchronous circuits and systems. *Journal of Circuits Systems and Computers*, 8(1):67–118, 1998.
- [33] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. A region-based theory for state assignment in speed-independent circuits. *IEEE Transactions on Computer-Aided Design*, 16(8):793–812, August 1997.
- [34] Tomás Lang, Enric Musoll, and Jordi Cortadella. Individual flip-flops with gated clocks for low-power datapaths. *IEEE Transactions on Circuits and Systems II*, 44(6):507–516, June 1997.

- [35] J. Cortadella, M. Kishinevsky, A.Kondratyev, L. Lavagno, and A. Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. *IEICE Transactions on Information and Systems*, E80-D(3):315–325, March 1997.
- [36] Jordi Cortadella and Tomás Lang. High-radix division and square root with speculation. *IEEE Transactions on Computers*, 43(8):919–931, August 1994.
- [37] Fermín Sánchez and Jordi Cortadella. Resource-constrained pipelining based on loop transformations. *Microprocessing and Microprogramming*, 38(1–5):429–436, September 1993.
- [38] Rosa M. Badia and Jordi Cortadella. GLASS: a graph-theoretic approach for global binding. *Microprocessing and Microprogramming*, 38(1–5):775–782, September 1993.
- [39] Jordi Cortadella and José M. Llabería. Evaluation of $A + B = K$ conditions without carry propagation. *IEEE Transactions on Computers*, 41(11):1484–1488, November 1992.
- [40] Jordi Cortadella and Teodor Jové. Comments on "Using Cache Mechanisms to Exploit non-Refreshing DRAM's for On-Chip Memories". *IEEE Journal of Solid-State Circuits*, 27(1):132, January 1992.
- [41] Jordi Cortadella, Rosa M. Badia, and Eduard Ayguadé. Scheduling in a continuous area-time design space. *Microprocessing and Microprogramming*, 32(1–5):199–206, August 1991.
- [42] Teodor Jové and Jordi Cortadella. Reduced instruction buffer for RISC architectures. *Microprocessing and Microprogramming*, 27(1–5):1987–1993, August 1989.
- [43] Jordi Cortadella and José M. Llabería. Making branches transparent to the execution unit. *International Journal of Mini and Microcomputers*, 11(1):13–17, January 1989.
- [44] Jordi Cortadella and Teodor Jové. Dynamic RAM for on-chip instruction caches. *Computer Architecture News*, 16(4):45–50, September 1988.
- [45] Antonio González, José M. Llabería, and Jordi Cortadella. A mechanism for reducing the cost of branches in RISC architectures. *Microprocessing and Microprogramming*, 24(1–5):565–572, August 1988.
- [46] Jordi Cortadella and Teodor Jové. Designing a branch target buffer for executing branches with zero time cost in a RISC processor. *Microprocessing and Microprogramming*, 24(1–5):573–580, August 1988.
- [47] Jordi Cortadella, Antonio González, and José M. Llabería. RISC: un nuevo enfoque en el diseño de procesadores. *Mundo electrónico*, 180:49–57, January 1988.

10.3 Conferences

- [1] M. Galceran-Oms, J. Cortadella, and M. Kishinevsky. Symbolic performance analysis of elastic systems. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 778–785, November 2010.
- [2] J. Carmona and J. Cortadella. Process mining meets abstract interpretation. In *Proc. European Conference on Machine Learning and Principles and Practice of Knowledge Discovery in Databases (ECML PKDD)*, volume 6321 of *Lecture Notes in Artificial Intelligence*, pages 184–199. Springer-Verlag, September 2010.
- [3] J. Cortadella, M. Galceran-Oms, and M. Kishinevsky. Elastic systems. In *Proc. 8th ACM/IEEE Int. Conf. on Formal Methods and Models for Codesign (MEMOCODE 2010)*, pages 149–158, July 2010.
- [4] J. Cortadella, L. Lavagno, D. Amiri, J. Casanova, C. Macián, F. Martorell, J.A. Moya, L. Necchi, D. Sokolov, and E. Tuncer. Narrowing the margins with elastic clocks. In *Proc. IEEE Int. Conf. on Integrated Circuit design and Technology*, pages 146–150, June 2010.

- [5] N. Nikitin, S. Chatterjee, J. Cortadella, M. Kishinevsky, and U. Ogras. Physical-aware link allocation and route assignment for chip multiprocessing. In *Proc. 4th ACM/IEEE Int. Symp. on Networks-on-Chip (NOCS)*, pages 125–134, May 2010.
- [6] M. Galceran-Oms, J. Cortadella, M. Kishinevsky, and D. Buřistov. Automatic microarchitectural pipelining. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 961–964, April 2010.
- [7] N. Nikitin and J. Cortadella. A performance analytical model for Network-on-Chip with constant service time routers. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 571–578, November 2009.
- [8] J. Casanova and J. Cortadella. Multi-level clustering for clock skew optimization. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 547–554, November 2009.
- [9] J. Carmona, J. Cortadella, and M. Kishinevsky. Divide-and-conquer strategies for process mining. In *Proc. 7th Int. Conf. Business Process Management*, volume 5701 of *Lecture Notes in Computer Science*, pages 327–343. Springer-Verlag, September 2009.
- [10] D. Buřistov, J. Cortadella, M. Galceran-Oms, J. Júlvez, and M. Kishinevsky. Retiming and recycling for elastic systems with early evaluation. In *Proc. ACM/IEEE Design Automation Conference*, pages 288–291, July 2009.
- [11] M. Galceran-Oms, J. Cortadella, and M. Kishinevsky. Speculation in elastic systems. In *Proc. ACM/IEEE Design Automation Conference*, pages 292–295, July 2009.
- [12] E. Tuncer, J. Cortadella, and L. Lavagno. Enabling adaptability through elastic clocks. In *Proc. ACM/IEEE Design Automation Conference*, pages 8–10, July 2009.
- [13] J. Carmona, J. Júlvez, J. Cortadella, and M. Kishinevsky. Scheduling synchronous elastic designs. In *Int. Conf. on Application of Concurrency to System Design*, June 2009. **Best paper award.**
- [14] M. Galceran-Oms, J. Cortadella, M. Kishinevsky, and D. Buřistov. Automatic microarchitectural pipelining. In *Proc. International Workshop on Logic Synthesis*, pages 214–221, June 2009.
- [15] D. Baneres, J. Cortadella, and M. Kishinevsky. Timing-driven n-way decomposition. In *Proc. of the Great Lakes Symposium on VLSI*, pages 363–368, May 2009.
- [16] D. Baneres, J. Cortadella, and M. Kishinevsky. Variable-latency design by function speculation. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 1704–1709, March 2009.
- [17] D. Buřistov, J. Júlvez, and J. Cortadella. Performance optimization of elastic systems using buffer resizing and buffer insertion. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 442–448, November 2008.
- [18] T. Kam, M. Kishinevsky, J. Cortadella, and M. Galceran-Oms. Correct-by-construction microarchitectural pipelining. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 434–441, November 2008.
- [19] K. Gorgônio and J. Cortadella. Hardware synthesis for asynchronous communications mechanisms. In *Int. Conf. of the Chilean Computer Science Society (SCCC)*, pages 135–143, November 2008.
- [20] A. Ziyatdinov, D. Bañeres, and J. Cortadella. Multi-clustering net model for placement algorithms. In *Proc. 16th IFIP/IEEE Int. Conf. on Very Large Scale Integration*, October 2008.
- [21] J. Carmona, J. Cortadella, and M. Kishinevsky. A region-based algorithm for discovering Petri nets from event logs. In *Proc. 6th Int. Conf. on Business Process Management (BPM)*, volume 5240 of *Lecture Notes in Computer Science*, pages 358–373. Springer-Verlag, September 2008.
- [22] J. Carmona, J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. A symbolic algorithm for the synthesis of bounded Petri nets. In *Applications and Theory of Petri Nets and Other Models of Concurrency (ICATPN)*, volume 5062 of *Lecture Notes in Computer Science*, pages 92–111. Springer-Verlag, June 2008.

- [23] D. Bufistov, J. Cortadella, M. Kishinevsky, and S. Sapatnekar. A general model for performance optimization of sequential systems. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 362–369, November 2007.
- [24] K. Gorgônio, J. Cortadella, and F. Xia. A compositional method for the synthesis of asynchronous communication mechanisms. In *Applications and Theory of Petri Nets and Other Models of Concurrency (ICATPN)*, volume 4546 of *Lecture Notes in Computer Science*, pages 144–163. Springer-Verlag, June 2007.
- [25] J. Cortadella and M. Kishinevsky. Synchronous elastic circuits with early evaluation and token counterflow. In *Proc. ACM/IEEE Design Automation Conference*, pages 416–419, June 2007.
- [26] D. Bañeres, J. Cortadella, and M. Kishinevsky. Layout-aware gate duplication and buffer insertion. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 1367–1372, April 2007.
- [27] S. Krstić, J. Cortadella, M. Kishinevsky, and J. O’Leary. Synchronous elastic networks. In *International Conference on Formal Methods in Computer-Aided Design (FMCAD)*, November 2006.
- [28] J. Carmona, J. Cortadella, Y. Takada, and F. Peper. From molecular interactions to gates: a systematic approach. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, November 2006.
- [29] J. Júlvez, J. Cortadella, and M. Kishinevsky. Performance analysis of concurrent systems with early evaluation. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, November 2006.
- [30] J. Carmona and J. Cortadella. State encoding of large asynchronous controllers. In *Proc. ACM/IEEE Design Automation Conference*, pages 939–944, July 2006.
- [31] J. Cortadella, M. Kishinevsky, and B. Grundmann. Synthesis of synchronous elastic architectures. In *Proc. ACM/IEEE Design Automation Conference*, pages 657–662, July 2006.
- [32] D. Bañeres, J. Cortadella, and M. Kishinevsky. Dominator-based partitioning for delay optimization. In *Proc. of the Great Lakes Symposium on VLSI*, pages 67–72, April 2006.
- [33] S. Krstić, J. Cortadella, M. Kishinevsky, and J. O’Leary. Synchronous elastic networks. In Mary Sheeran and Tom Melham, editors, *Sixth International Workshop on Designing Correct Circuits (DCC)*. ETAPS 2006, March 2006.
- [34] J. Cortadella, M. Kishinevsky, and B. Grundmann. Specification and design of synchronous elastic circuits. In *Proc. International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, pages 16–21, February 2006.
- [35] R. Clarisó and J. Cortadella. Verification of concurrent systems with parametric delays using octahedra. In *Int. Conf. on Application of Concurrency to System Design*, pages 122–131, June 2005.
- [36] J. Cortadella, K. Gorgônio, F. Xia, and A. Yakovlev. Automatic synthesis of asynchronous communication mechanisms. In *Int. Conf. on Application of Concurrency to System Design*, pages 166–175, June 2005.
- [37] R. Clarisó, E. Rodríguez-Carbonell, and J. Cortadella. Derivation of non-structural invariants of Petri nets using abstract interpretation. In *Application and Theory of Petri Nets 2004*, volume 3536 of *Lecture Notes in Computer Science*, pages 188–207. Springer-Verlag, June 2005.
- [38] E. Rodríguez-Carbonell and J. Cortadella. Inference of numerical relations from digital circuits. Extended abstract of the presentation at the First International Workshop on Numerical & Symbolic Abstract Domains (NSAD), January 2005.
- [39] J. Cortadella, A. Kondratyev, L. Lavagno, and C. Sotiriou. Coping with the variability of combinational logic delays. In *Proc. International Conf. Computer Design (ICCD)*, pages 505–508, October 2004.

- [40] Robert Clarisó and Jordi Cortadella. The octahedron abstract domain. In *11th Static Analysis Symposium (SAS)*, volume 3148 of *Lecture Notes in Computer Science*, pages 312–327. Springer-Verlag, August 2004.
- [41] D. Bañeres, J. Cortadella, and M. Kishinevsky. A recursive paradigm to solve boolean relations. In *Proc. ACM/IEEE Design Automation Conference*, pages 416–421, June 2004. **Best paper award.**
- [42] I. Blunno, J. Cortadella, A. Kondratyev, L. Lavagno, K. Lwin, and C. Sotiriou. Handshake protocols for de-synchronization. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 149–158, April 2004. **Best paper award.**
- [43] J. Cortadella, A. Kondratyev, L. Lavagno, K. Lwin, and C. Sotiriou. From synchronous to asynchronous: An automatic approach. In *Proc. Design, Automation and Test in Europe (DATE)*, volume 2, pages 1368–1369, February 2004.
- [44] R. Clarisó and J. Cortadella. Verification of timed circuits with symbolic delays. In *Proc. of Asia and South Pacific Design Automation Conference*, pages 628–633, January 2004.
- [45] N. Modi and J. Cortadella. Boolean decomposition using two-literal divisors. In *Proc. International Conference on VLSI Design*, January 2004.
- [46] J. Carmona and J. Cortadella. ILP models for the synthesis of asynchronous control circuits. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 818–825, November 2003.
- [47] J. Cortadella, A. Kondratyev, L. Lavagno, and Y. Watanabe. Quasi-static scheduling for concurrent architectures. In *Int. Conf. on Application of Concurrency to System Design*, pages 29–40, June 2003.
- [48] J. Cortadella, A. Kondratyev, L. Lavagno, and C. Sotiriou. A concurrent model for de-synchronization. In *Proc. International Workshop on Logic Synthesis*, pages 294–301, May 2003.
- [49] R. Clarisó and J. Cortadella. Verification of timed circuits with symbolic delays. In *Proc. International Workshop on Logic Synthesis*, pages 310–317, May 2003.
- [50] J. Carmona and J. Cortadella. Input/output compatibility of reactive systems. In M. Aagaard and J.W. O’Leary, editors, *International Conference on Formal Methods in Computer-Aided Design (FMCAD)*, volume 2517 of *Lecture Notes in Computer Science*, pages 360–377. Springer-Verlag, November 2002.
- [51] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Claudio Passerone, and Yosinori Watanabe. Quasi-static scheduling of independent tasks for reactive systems. In *Application and Theory of Petri Nets 2002*, volume 2360 of *Lecture Notes in Computer Science*, pages 80–99. Springer-Verlag, June 2002.
- [52] J. Cortadella. Bi-decomposition and tree-height reduction for timing optimization. In *Proc. International Workshop on Logic Synthesis*, June 2002.
- [53] R. Clarisó, J. Cortadella, A. Kondratyev, L. Lavagno, C. Passerone, and Y. Watanabe. Synthesis of embedded software for reactive systems. In *Int. Workshop on Integration of Specification Techniques for Applications in Engineering (Satellite event of ETAPS 2002)*, pages 2–20, April 2002.
- [54] M.A. Peña, J. Cortadella, E. Pastor, and A. Smirnov. A case study for the verification of complex timed circuits: IPCMOS. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 44–51, March 2002.
- [55] G. Cornetta and J. Cortadella. Asynchronous multipliers with variable-delay counters. In *8th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)*, volume II, pages 701–705, September 2001.
- [56] Josep Carmona, Jordi Cortadella, and Enric Pastor. A structural encoding technique for the synthesis of asynchronous circuits. In *Int. Conf. on Application of Concurrency to System Design*, pages 157–166, June 2001.
- [57] Gianluca Cornetta and Jordi Cortadella. A multi-radix approach to asynchronous division. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 25–34, March 2001.

- [58] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Hardware and Petri nets: Application to asynchronous circuit design. In *Application and Theory of Petri Nets 2000*, volume 1825 of *Lecture Notes in Computer Science*, pages 1–15. Springer-Verlag, June 2000.
- [59] Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Marc Massot, Sandra Moral, Claudio Passerone, Yosinori Watanabe, and Alberto Sangiovanni-Vincentelli. Task generation and compile-time scheduling for mixed data-control embedded software. In *Proc. ACM/IEEE Design Automation Conference*, pages 489–494, June 2000.
- [60] Marco A. Peña, Jordi Cortadella, Alex Kondratyev, and Enric Pastor. Formal verification of safety properties in timed circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 2–11, April 2000.
- [61] Jordi Cortadella and Gabriel Valiente. A relational view of subgraph isomorphism. In *Proc. International Seminar on Relational Methods in Computer Science*, pages 45–54, January 2000.
- [62] Hiroshi Saito, Alex Kondratyev, Jordi Cortadella, Luciano Lavagno, and Alexander Yakovlev. What is the cost of delay insensitivity? In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 316–323, November 1999.
- [63] Jordi Cortadella, Michael Kishinevsky, Steven M. Burns, and Ken Stevens. Synthesis of asynchronous control circuits with automatically generated timing assumptions. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 324–331, November 1999.
- [64] Hiroshi Saito, Alex Kondratyev, Jordi Cortadella, Luciano Lavagno, and Alexander Yakovlev. Bridging modularity and optimality: delay-insensitive interfacing in asynchronous circuits synthesis. In *Proc. IEEE International Conference on Systems, Man and Cybernetics (SMC)*, volume 3, pages 899–904, October 1999.
- [65] Enric Pastor, Jordi Cortadella, and Marco A. Peña. Structural Methods to Improve the Symbolic Analysis of Petri Nets. In *Application and Theory of Petri Nets 1999*, volume 1639 of *Lecture Notes in Computer Science*, pages 26–45. Springer-Verlag, June 1999.
- [66] Ken Stevens, Shai Rotem, Steven M. Burns, Jordi Cortadella, Ran Ginosar, Michael Kishinevsky, and Marly Roncken. CAD directions for high performance asynchronous circuits. In *Proc. ACM/IEEE Design Automation Conference*, pages 116–121, June 1999.
- [67] Alex Kondratyev, Jordi Cortadella, Michael Kishinevsky, Luciano Lavagno, and Alexander Yakovlev. Automatic synthesis and optimization of partially specified asynchronous systems. In *Proc. ACM/IEEE Design Automation Conference*, pages 110–115, June 1999.
- [68] Hiroshi Saito, Alex Kondratyev, Jordi Cortadella, Luciano Lavagno, and Alexander Yakovlev. What is the cost of delay insensitivity? In *Proc. of the Workshop Hardware Design and Petri Nets (within the International Conference on Application and Theory of Petri Nets)*, pages 169–189, June 1999.
- [69] A. Taubin, A. Kondratyev, J. Cortadella, and L. Lavagno. Behavioral transformations to increase the noise immunity of asynchronous specifications. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 36–47, April 1999.
- [70] Gianluca Cornetta and Jordi Cortadella. A radix-16 SRT division unit with speculation of quotient digits. In *Proc. of the Great Lakes Symposium on VLSI*, pages 74–77, March 1999.
- [71] A. Taubin, A. Kondratyev, J. Cortadella, and L. Lavagno. Crosstalk noise avoidance in asynchronous circuits. In *Proc. International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)*, pages 123–128, March 1999.
- [72] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, A. Taubin, and A. Yakovlev. Lazy transition systems: application to timing optimization of asynchronous circuits. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 324–331, November 1998.

- [73] Tomás Lang, Enric Musoll, and Jordi Cortadella. Extension of the working-zone-encoding method to reduce also the energy on the microprocessor data bus. In *Proc. International Conf. Computer Design (ICCD)*, pages 414–419, October 1998.
- [74] M. Kishinevsky, J. Cortadella, and A. Kondratyev. Asynchronous interface specification, analysis and synthesis. In *Proc. ACM/IEEE Design Automation Conference*, pages 2–7, June 1998.
- [75] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Automatic handshake expansion and reshuffling using concurrency reduction. In *Proc. of the Workshop Hardware Design and Petri Nets (within the International Conference on Application and Theory of Petri Nets)*, pages 86–110, June 1998.
- [76] Enric Pastor and Jordi Cortadella. Structural methods applied to the symbolic analysis of Petri nets. In *Proc. International Workshop on Logic Synthesis*, June 1998.
- [77] Enric Musoll, Tomás Lang, and Jordi Cortadella. Reducing the energy of address and data buses with the working-zone encoding technique and its effect on multimedia applications. In *Proc. of the Power Driven Microarchitecture Workshop*, pages 3–8, June 1998.
- [78] Jordi Cortadella. Combining structural and symbolic methods for the verification of concurrent systems. In *Int. Conf. on Application of Concurrency to System Design*, pages 2–7, March 1998.
- [79] A. Kondratyev, J. Cortadella, M. Kishinevsky, L. Lavagno, A. Taubin, and A. Yakovlev. Identifying state coding conflicts in asynchronous system specifications using Petri net unfoldings. In *Int. Conf. on Application of Concurrency to System Design*, pages 152–163, March 1998.
- [80] Enric Pastor and Jordi Cortadella. Efficient encoding schemes for symbolic analysis of Petri nets. In *Proc. Design, Automation and Test in Europe (DATE)*, pages 790–795, March 1998.
- [81] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, Enric Pastor, and Alexandre Yakovlev. Decomposition and technology mapping of speed-independent circuits using Boolean relations. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, November 1997.
- [82] Enric Musoll, Tomás Lang, and Jordi Cortadella. Exploiting the locality of memory references to reduce the address bus energy. In *International Symposium on Low Power Electronics and Design*, pages 202–207, August 1997.
- [83] Michael Kishinevsky, Jordi Cortadella, Alex Kondratyev, Luciano Lavagno, Alexander Taubin, and Alex Yakovlev. Coupling asynchrony and interrupts: Place chart nets and their synthesis. In Pierre Azéma and Gianfranco Balbo, editors, *Application and Theory of Petri Nets 1997*, volume 1248 of *Lecture Notes in Computer Science*, pages 328–347. Springer-Verlag, Toulouse, France, June 1997.
- [84] Oriol Roig, Jordi Cortadella, Marco A. Peña, and Enric Pastor. Automatic generation of synchronous test patterns for asynchronous circuits. In *Proc. ACM/IEEE Design Automation Conference*, pages 620–625, June 1997.
- [85] Alex Semenov, Alexandre Yakovlev, Enric Pastor, Marco A. Peña, and Jordi Cortadella. Synthesis of speed-independent circuits from STG-unfolding segment. In *Proc. ACM/IEEE Design Automation Conference*, pages 16–21, June 1997.
- [86] Jordi Cortadella, Luciano Lavagno, and Ellen Sentovich. Logic synthesis techniques for embedded control code optimization. In *Proc. International Workshop on Logic Synthesis*, June 1997.
- [87] Alex Semenov, Alexandre Yakovlev, Enric Pastor, Marco A. Peña, Jordi Cortadella, and Luciano Lavagno. Partial order based approach to synthesis of speed-independent circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 254–265. IEEE Computer Society Press, April 1997.

- [88] Alex Kondratyev, Michael Kishinevsky, Jordi Cortadella, Luciano Lavagno, and Alex Yakovlev. Technology mapping for speed-independent circuits: decomposition and resynthesis. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 240–253. IEEE Computer Society Press, April 1997.
- [89] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alex Yakovlev. Technology mapping of speed-independent circuits based on combinational decomposition and resynthesis. In *Proc. European Design and Test Conference*, pages 98–105, 1997.
- [90] Luciano Lavagno, Jordi Cortadella, and Alberto Sangiovanni-Vincentelli. Embedded code optimization via common control structure detection. In *International Workshop on Hardware/Software Co-Design (Codes/CASHE)*, March 1997.
- [91] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. In *XI Conference on Design of Integrated Circuits and Systems*, pages 205–210, Barcelona, November 1996.
- [92] Tomás Lang, Enric Musoll, and Jordi Cortadella. Redundant adder for reduced output transitions. In *XI Conference on Design of Integrated Circuits and Systems*, pages 17–22, Barcelona, November 1996.
- [93] Jordi Cortadella, Rosa M. Badia, and Fermín Sánchez. A mathematical formulation of the loop pipelining problem. In *XI Conference on Design of Integrated Circuits and Systems*, pages 355–360, Barcelona, November 1996.
- [94] L. Sintes, J. Escudero, M.A. Peña, O. Roig, J. Cortadella, and J. Carrabina. Flujo de diseño asíncrono con la biblioteca DCVSL_LIB para ES2 ECPD10. In *Actas del II Congreso sobre Tecnologías Aplicadas a la Enseñanza de la Electrónica*, pages 161–166, Sevilla, September 1996.
- [95] Fermín Sánchez and Jordi Cortadella. RESIS: A new methodology for register optimization in software pipelining. In *Proc. European Conference on Parallel Processing (EURO-PAR)*, August 1996.
- [96] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alex Yakovlev. Methodology and tools for state encoding in asynchronous circuit synthesis. In *Proc. ACM/IEEE Design Automation Conference*, 1996.
- [97] Fermín Sánchez and Jordi Cortadella. Maximum-throughput software pipelining. In *Proc. International Conference on Massively Parallel Computing Systems*, pages 483–490, May 1996.
- [98] M. A. Peña and J. Cortadella. Combining process algebras and Petri nets for the specification and synthesis of asynchronous circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*. IEEE Computer Society Press, March 1996.
- [99] Enric Musoll and Jordi Cortadella. Optimizing CMOS circuits for low power using transistor reordering. In *Proc. European Design and Test Conference*, pages 222–232, March 1996.
- [100] E. Pastor, J. Cortadella, O. Roig, and A. Kondratyev. Structural methods for the synthesis of speed-independent circuits. In *Proc. European Design and Test Conference*, pages 340–347. IEEE Computer Society Press, March 1996.
- [101] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Complete state encoding based on the theory of regions. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*. IEEE Computer Society Press, March 1996.
- [102] Enric Pastor and Jordi Cortadella. Cover approximations for the synthesis of speed-independent circuits. In *Proc. of the IFIP International Workshop on Logic and Architecture Synthesis*, pages 150–159, December 1995.

- [103] Marco A. Peña and Jordi Cortadella. Programación VLSI y síntesis de circuitos asíncronos mediante composición de redes de Petri. In *Actas del X Congreso de Diseño de Circuitos Integrados y Sistemas*, pages 65–70, Zaragoza, November 1995.
- [104] J. Cortadella, M. Kishinevsky, L. Lavagno, and A. Yakovlev. Synthesizing Petri nets from state-based models. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 164–171, 1995.
- [105] F. Sanchez and J. Cortadella. Time constrained loop pipelining. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 592–596, November 1995.
- [106] Enric Musoll and Jordi Cortadella. Low-power array multipliers with transition-retaining barriers. In *Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pages 227–238, October 1995.
- [107] Enric Musoll and Jordi Cortadella. Scheduling and resource binding for low power. In *International Symposium on System Synthesis*, pages 104–109, September 1995.
- [108] Oriol Roig, Jordi Cortadella, and Enric Pastor. Verification of asynchronous circuits by BDD-based model checking of Petri nets. In *Application and Theory of Petri Nets 1995*, volume 815 of *Lecture Notes in Computer Science*, pages 374–391. Springer-Verlag, June 1995.
- [109] Oriol Roig, Jordi Cortadella, and Enric Pastor. Hierarchical gate-level verification of speed-independent circuits. In *Asynchronous Design Methodologies*, pages 129–137. IEEE Computer Society Press, May 1995.
- [110] Enric Musoll and Jordi Cortadella. High-level synthesis techniques for reducing the activity of functional units. In *International Symposium on Low Power Design*, pages 94–104, April 1995.
- [111] Enric Pastor, Jordi Cortadella, and Oriol Roig. A new look at the conditions for the synthesis of speed-independent circuits. In *Proc. of the Great Lakes Symposium on VLSI*, pages 230–235, March 1995.
- [112] A. Kondratyev, J. Cortadella, M. Kishinevsky, E. Pastor, O. Roig, and A. Yakovlev. Checking Signal Transition Graph implementability by symbolic BDD traversal. In *Proc. European Design and Test Conference*, pages 325–332, Paris, France, March 1995.
- [113] Jordi Cortadella, Luciano Lavagno, Peter Vanbekbergen, and Alexandre Yakovlev. Designing asynchronous circuits from behavioral specifications with internal conflicts. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 106–115, November 1994.
- [114] Oriol Roig, Enric Pastor, and Jordi Cortadella. Verificación de circuitos independientes de la velocidad con modelos simbólicos de redes de Petri. In *Actas del IX Congreso de Diseño de Circuitos Integrados y Sistemas*, pages 307–312, Gran Canaria, November 1994.
- [115] Enric Pastor, Oriol Roig, Jordi Cortadella, and Rosa M. Badia. Petri net analysis using boolean manipulation. In *Application and Theory of Petri Nets 1994*, volume 815 of *Lecture Notes in Computer Science*, pages 416–435. Springer-Verlag, June 1994.
- [116] J. Cortadella, J.A.B. Fortes, and E.A. Lee. Design and prototyping of digital signal processing systems (mini-track introduction). In *Proc. Hawaii International Conf. System Sciences*, pages 56–57, January 1994.
- [117] Enric Pastor and Jordi Cortadella. Polynomial algorithms for the synthesis of hazard-free circuits from signal transition graphs. In *Proc. International Conf. Computer-Aided Design (ICCAD)*, pages 250–254. IEEE Computer Society Press, November 1993.
- [118] Oriol Roig, Enric Pastor, Rosa M. Badia, and Jordi Cortadella. Síntesis de máquinas de control para circuitos asíncronos. In *Actas del VIII Congreso de Diseño de Circuitos Integrados y Sistemas*, pages 326–331, Málaga, November 1993.
- [119] Enric Pastor and Jordi Cortadella. An efficient unique state coding algorithm for signal transition graphs. In *Proc. International Conf. Computer Design (ICCD)*, pages 174–177, October 1993.

- [120] Jordi Cortadella and Tomás Lang. Division with speculation of quotient digits. In *International Symposium on Computer Arithmetic*, pages 87–94, June 1993.
- [121] Rosa M. Badia and Jordi Cortadella. High-level synthesis of asynchronous systems: Scheduling and process synchronization. In *Proc. European Conference on Design Automation (EDAC)*, pages 70–74. IEEE Computer Society Press, February 1993.
- [122] Jordi Cortadella, Rosa M. Badia, Enric Pastor, and Abelardo Pardo. Achilles: A high-level synthesis system for asynchronous circuits. In *6th ACM/IEEE International Workshop on High-Level Synthesis*, pages 87–94, November 1992.
- [123] Jordi Cortadella, Rosa M. Badia, Enric Pastor, and Abelardo Pardo. Achilles: Sistema de síntesis de alto nivel para circuitos asíncronos. In *Actas del VII Congreso de Diseño de Circuitos Integrados y Sistemas*, pages 357–362, Toledo, November 1992.
- [124] J. Cortadella and R. M. Badia. An asynchronous architecture model for behavioral synthesis. In *Proc. European Conference on Design Automation (EDAC)*, pages 307–311. IEEE Computer Society Press, March 1992.
- [125] Rosa M. Badia and Jordi Cortadella. Optimización del tiempo de ciclo en la planificación de operaciones. In *Actas del VI Congreso de Diseño de Circuitos Integrados y Sistemas*, pages 275–280, Santander, November 1991.
- [126] G.S. Whitcomb, J. Cortadella, and A.R. Newton. Functional level synthesis of the TRISC processor. In *IFIP International Workshop on Application of Synthesis and Simulation*, August 1991.
- [127] Jordi Cortadella, Rosa M. Badia, and Eduard Ayguadé. Scheduling in a continuous area-time design space: A simulated-annealing-based approach. In *5th ACM/IEEE International Workshop on High-Level Synthesis*, pages 102–117, March 1991.
- [128] Rosa M. Badia, Jordi Cortadella, and Eduard Ayguadé. Computer-aided synthesis of data-path by using a simulated-annealing-based approach. In *9th IAESTED International Symposium on Applied Informatics*, pages 326–329, February 1991.
- [129] Jordi Cortadella and José M. Llabería. Evaluating $A+B = K$ conditions in constant time. In *Proc. International Symposium on Circuits and Systems*, pages 243–246, June 1988.
- [130] Jordi Cortadella and Teodor Jové. Executing zero-delay branches with a branch target buffer in a RISC processor. In *36th International Symposium on Mini and Microcomputers and their applications*, pages 373–376, June 1988.
- [131] Jordi Domingo, José M. Llabería, Mateo Valero, and Jordi Cortadella. Arbitration techniques for packet switching multistage networks. In *3rd. International Conference on Supercomputing*, volume III, pages 240–248, May 1988.
- [132] Jordi Cortadella. Executing branch instructions with zero time delay in a RISC. In *IEEE Computer Society Workshop on VLSI*, Clearwater Beach (Florida), February 1988.
- [133] Antonio González, José M. Llabería, and Jordi Cortadella. Zero-delay cost branches in RISC architectures. In *6th International Symposium on Applied Informatics*, pages 24–27, February 1988.
- [134] Jordi Cortadella and José M. Llabería. Arquitecturas RISC. In *IV Jornadas de Diseño Lógico*, pages 19–27, Barcelona, 1987.
- [135] Jordi Domingo, José M. Llabería, Jordi Cortadella, and Mateo Valero. Arbitration methods to increase the throughput of packed switching buffered shuffle-exchange interconnection networks. In *International Symposium on Applied Informatics*, pages 78–81, February 1987.

- [136] Jordi Cortadella and José M. Llabería. An intelligent IFU for pipelined processors that makes control instructions transparent to the execution unit. In *International Symposium on Applied Informatics*, pages 188–191, February 1987.
- [137] Jordi Cortadella and José M. Llabería. A low cost evaluation methodology for new architectures. In *International Symposium on Applied Informatics*, pages 188–191, February 1987.
- [138] Jordi Cortadella and José M. Llabería. Procesadores RISC. In *Ier. Seminario del grupo temático de Arquitectura y Tecnología de Ordenadores sobre Arquitecturas Multiprocesadores y sus Aplicaciones*, Madrid, January 1987.
- [139] Luis González, Jordi Cortadella, and José M. Llabería. Performance evaluation of a loosely coupled multiprocessor architecture with two buses. In *International Symposium on Mini and Microcomputers and their applications*, pages 473–476, June 1985.

11 Tutorials and invited lectures

- [1] J. Cortadella and M. Kishinevsky. Elasticity and Petri nets. Advanced tutorial at the 28th Int. Conf. on Application and Theory of Petri Nets, Siedlce, Poland, June 2007.
- [2] Michael Kishinevsky, Jordi Cortadella, Bill Grundmann, Sava Krstic, and John O’Leary. Synchronous elastic circuits. In Dima Grigoriev, John Harrison, and Edward A. Hirsch, editors, *Computer Science - Theory and Applications, First International Computer Science Symposium in Russia, CSR 2006, St. Petersburg, Russia, June 8-12, 2006, Proceedings*, volume 3967 of *Lecture Notes in Computer Science*, pages 3–5. Springer, 2006.
- [3] P.A. Beerel, J. Cortadella, and A. Kondratyev. Bridging the gap between asynchronous design and designers. Tutorial at the VLSI Design Conference, Mumbai, India, January 2004.
- [4] J. Cortadella and A. Yakovlev. Petrify. Hands-on tutorial at the Summer School on Asynchronous Circuit Design, (organized by the ACiD-WG, Grenoble), July 2002.
- [5] J. Cortadella, M. Kishinevsky, A. Kondratyev, L. Lavagno, and A. Yakovlev. Hazard free logic synthesis and technology mapping. Lecture at the Summer School on Asynchronous Circuit Design, (organized by the ACiD-WG, Grenoble), July 2002.
- [6] J. Cortadella. Synthesis of embedded software for reactive systems. Invited lecture at the Int. Workshop on Integration of Specification Techniques for Applications in Engineering (Satellite event of ETAPS 2002), April 2002.
- [7] J. Cortadella, A. Yakovlev, and J. Garside. Logic design of asynchronous circuits. Tutorial at the ASP-DAC/VLSI Design Conference, Bangalore, India, January 2002.
- [8] J. Cortadella. Tools for automatic synthesis and verification of asynchronous interfaces. Invited lecture at the workshop “Asynchronous Interfaces: Tools, techniques, and implementations” (AINT’2000), Delft, The Netherlands, July 2000.
- [9] Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Hardware and Petri nets: Application to asynchronous circuit design. Invited lecture at the 21st Int. Conf. on Application and Theory of Petri Nets, Aarhus, Denmark, June 2000.
- [10] J. Cortadella, L. Lavagno, and A. Yakovlev. Hardware design and Petri nets. Advanced tutorial at the 21st Int. Conf. on Application and Theory of Petri Nets, Aarhus, Denmark, June 2000.
- [11] J. Cortadella, M. Kishinevsky, A. Kondratyev, and L. Lavagno. Introduction to asynchronous circuit design: specification and synthesis. Tutorial at the 6th Int. Symp. on Advanced Research in Asynchronous Circuits and Systems, Eilat, Israel, April 2000.

- [12] J. Cortadella. STG-based synthesis and petrify. Tutorial at the 3rd ACiD-WG Workshop, Newcastle upon Tyne, UK, January 1999.
- [13] M. Kishinevsky, J. Cortadella, and A. Kondratyev. Asynchronous interface specification, analysis and synthesis. Embedded tutorial at the Design Automation Conference, San Francisco, USA, June 1998.
- [14] J. Cortadella. Asynchronous circuit verification and synthesis with Petri nets. Invited lecture at the Workshop on Hardware Design and Petri Nets , Lisbon, June 1998.
- [15] J. Cortadella. Combining structural and symbolic methods for the verification of concurrent systems. Invited lecture at the International Conference on Application of Concurrency to System Design (CSD'98), Aizu-Wakamatsu, Japan, March 1998.
- [16] J. Cortadella and M. Kishinevsky. Synthesis of control circuits from STG specifications. Course in the Summer School on Asynchronous Circuit Design (organized by the ACiD-WG, ESPRIT 21949), Lyngby, Denmark, August 1997.
- [17] J. Cortadella, E. Macii, G. De Micheli, M. Pedram, J. Rabaey, and K. van Berkel. What's hot in low power design ? Participation at the panel session at the European Design Automation Conference (EURO-DAC), Geneve, Switzerland, September 1996.
- [18] J. Cortadella. Executing branch instructions with zero time delay in a RISC. Invited lecture at the IEEE Computer Society Workshop on VLSI, Clearwater Beach, USA, February 1988.
- [19] J. Cortadella. Arquitecturas RISC. Invited lecture at the IV Jornadas de Diseño Lógico, Barcelona, 1987.